Exhibit 9

JEDEC STANDARD

DDR4 Registering Clock Driver Definition (DDR4RCD02)

JESD82-31A

(Revision of JESD82-31, August 2016)

AUGUST 2019

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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DDR4 REGISTER DEFINITION (DDR4RCD02)

(From JEDEC Board Ballot, JCB-17-02, formulated under the cognizance of the JC-40.4 Subcommittee on Registered and Fully Buffered Memory Support Logic.)

1 Scope

This document defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the DDR4 Registering Clock Driver (RCD) with parity for driving address and control nets on DDR4 RDIMM and LRDIMM applications.

The terms 'Registering Clock Driver', 'RCD', 'register' or 'device' are used interchangeably to refer to this device in the remainder of this standard.

The purpose is to provide a standard for the DDR4RCD02 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

NOTE The designation DDR4RCD02 refers to the part designation of a series of commercial logic parts common in the industry. This designation is normally preceded by a series of manufacturer specific characters to make up a complete part designation.

2 Device standard

2.1 Description

This 32-bit 1:2 registering clock driver with parity is designed for 1.2 V V_{DD} operation.

All inputs are pseudo-differential with an external or internal voltage reference. All outputs are full swing CMOS drivers optimized to drive single terminated 25 Ω to 50 Ω traces in DDR4 RDIMM and LRDIMM applications. Clock outputs Yn_t and Yn_c, and the control net outputs QxCKEn, QxCSn and QxODTn can be driven with a different strengths to compensate for different DIMM net topologies. By disabling unused outputs the power consumption is reduced.

The DDR4RCD02 operates from a differential clock (CK_t/CK_c). Inputs are registered at the crossing of CK_t going HIGH, and CK_c going LOW. The input signals could be either re-driven to the outputs or they could be used to access device internal control registers when certain input conditions are met. The control word mechanism is described in more detail in “Control Word Decoding” on page 69.

2.2 Features and Functions

The DDR4RCD02 has three basic modes of operation associated with the DA[1:0] bits in the DIMM Configuration Control Word (F0RC0D):

- In **Direct DualCS mode** (DA[1:0] = 00) the component has two chip select inputs, DCS0_n and DCS1_n, and two copies of each chip select output, QACS0_n, QACS1_n, QBCS0_n and QBCS1_n. The inputs pins DC[2:0] are forwarded to two sets of output pins, QAC[2:0] and QBC[2:0]. This is the normal operating mode (“QuadCS disabled” and “Encoded CS disabled”).
- In **Direct QuadCS mode** (DA[1:0] = 01), the component has four chip select inputs, the two dedicated inputs DCS[1:0]_n and the DC[0] input pin functioning as DCS2_n and the DC[1] input pin functioning as DCS3_n, and two copies of each chip select output, QACS[3:0]_n and QBCS[3:0]_n. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the “QuadCS enabled” mode.

  In the two modes above the DDR4RCD02 does not need to decode input signals to generate any chip select outputs.
- In **Encoded QuadCS mode** (DA[1:0] = 11), two copies of four output chip selects, i.e. QACS[3:0]_n and QBCS[3:0]_n, are decoded out of two DCS[1:0]_n inputs and the DC[0] input. The input pin DC[2] is forwarded to two output pins, QAC[2] and QBC[2]. The output pins QAC[1:0] and QBC[1:0] are used as QACS[3:2]_n and QBCS[3:2]_n. This is the “Encoded QuadCS” mode.

When the DCS encoding is changed (i.e. when the setting in F0RC0D DA[1:0] is updated), it is necessary for the host to precondition the signals driven on the pins which will be turned into chip select inputs with the correct voltage levels. For example, it is necessary to drive DCS[3:2] both HIGH before F0RC0D DA[1:0] is updated from ‘00’ to ‘01’. This is necessary to prevent a violation of the t_{MRD} parameter.

Through the remainder of this specification, DCS[n:0]_n will indicate all of the chip select inputs, where n=1 for

RCD0D DA0=0, and n=3 for RCD0D DA0=1. QxCS[n:0]_n will indicate all of the chip select outputs.

Table 1 — Generic DCS - QxCS Mapping

Input CS	Output CS		
	Direct DualCS mode	Direct QuadCS mode	Encoded QuadCS mode
DCS0_n	QxCS0_n	QxCS0_n	QxCS0_n, QxCS1_n
DCS1_n	QxCS1_n	QxCS1_n	QxCS2_n, QxCS3_n
DCS2_n/DC0	n/a	QxCS2_n	n/a
DCS3_n/DC1	n/a	QxCS3_n	n/a

2.2.1 Direct CS Modes

Commands are sent to a single rank or multiple ranks, as determined by the DCS[n:0]_n and DC[n:0] inputs. The number of input chip selects matches the number of output chip selects in each of the two sets (A-outputs and B-outputs).

The number of input chip selects is two (in Direct DualCS mode) or four (in Direct QuadCS mode).

2.2.2 Quad CS Modes

For DIMMs using dual-die packages there is a need for four CS signals rather than the standard two. For these modules two modes are available where four CS outputs are available. The memory controller can select by programming the CS mode control bits which of the two modes it wants to utilize.

There are two ways of accomplishing this:

- by using four CS inputs from the host (DCS[3:0]_n). This is the Direct QuadCS mode. See Chapter 2.2.1, “Direct CS Modes,” above.
- by using two CS inputs and one of the chip ID inputs from the host (DCS[1:0]_n and DC0). See Chapter 2.2.3, “Encoded QuadCS Mode,” below.

2.2.3 Encoded QuadCS Mode

When F0RC0D DA[1:0] = 11 the DDR4 register decodes two sets of four QxCS_n outputs from two DCS_n inputs by using the DC0 as the encoding input.

Table 2 — DCS, DC - QxCS, QxC Mapping in Encoded QuadCS mode

DCS1_n	DCS0_n	DC0	DC2	QxCS[3:0]_n	QxC2
H	H	X	0	HHHH	No change
		X	1		
H	L	0	0	HHHL	0
		0	1		1
		1	0	HHLH	0
		1	1		1
L	H	0	0	HLHH	0
		0	1		1
		1	0	LHHH	0
		1	1		1
L	L	0	0	HLHL[1]	0
		0	1		1
		1	0	LHLH[1]	0
		1	1		1

1.Only one DCSx_n input can be asserted for DRAM MRS and DRAM read commands

No additional address bits are used.

All commands including read, write, precharge, refresh and MRS commands are sent to the rank selected by the two chip selects and chip ID bit 0 coming from the host.

The memory controller needs to handle commands in the same way it would handle a DIMM with two times as many chip selects.

2.3 Initialization

To ensure defined outputs from the register before a stable clock has been supplied, the register must enter the reset state during power-up. After the voltage ramp, stable power is provided for a minimum of 200 µS with DRST_n asserted. When the reset input DRST_n is LOW, all input receivers are disabled, and can be left floating. Since internally generated Vref is selected in F0RC0B DA3 for Input Receiver Vref source after DRST_n is driven LOW, the reference voltage (VrefCA) doesn't need to be stable. In addition, when DRST_n is LOW, all control registers are restored to their default states, which is all '0's unless explicitly stated otherwise. The outputs QRST_n, QACKE0, QACKE1, QBCKE0 and QBCKE1 and BCK_t/BCK_c must drive LOW and BCKE must drive HIGH during reset. All other Qx outputs must float. As long as the DRST_n input is pulled LOW the register is in low power state and input termination is not present. A certain period of time (t_{ACT}) before the DRST_n input is pulled HIGH the clock input signal must be stable, the register inputs DCKE0 and DCKE1 must be pulled LOW. After reset and after the stabilization time (t_{STAB}) the register must meet the input Setup and Hold specification, as well as accept and transfer input signals to the corresponding outputs. The DRST_n input must always be held at a valid logic level once the input clock is present.

To ensure defined outputs from the register before a stable clock has been supplied, the register must enter the reset state during power-up. It may leave this state only after a LOW to HIGH transition on DRST_n while a stable clock signal is present on CK_t and CK_c. In the DDR4 RDIMM and LRDIMM applications, DRST_n is specified to be completely asynchronous with respect to CK_c and CK_t. Therefore, no timing relationship can be guaranteed between the two.

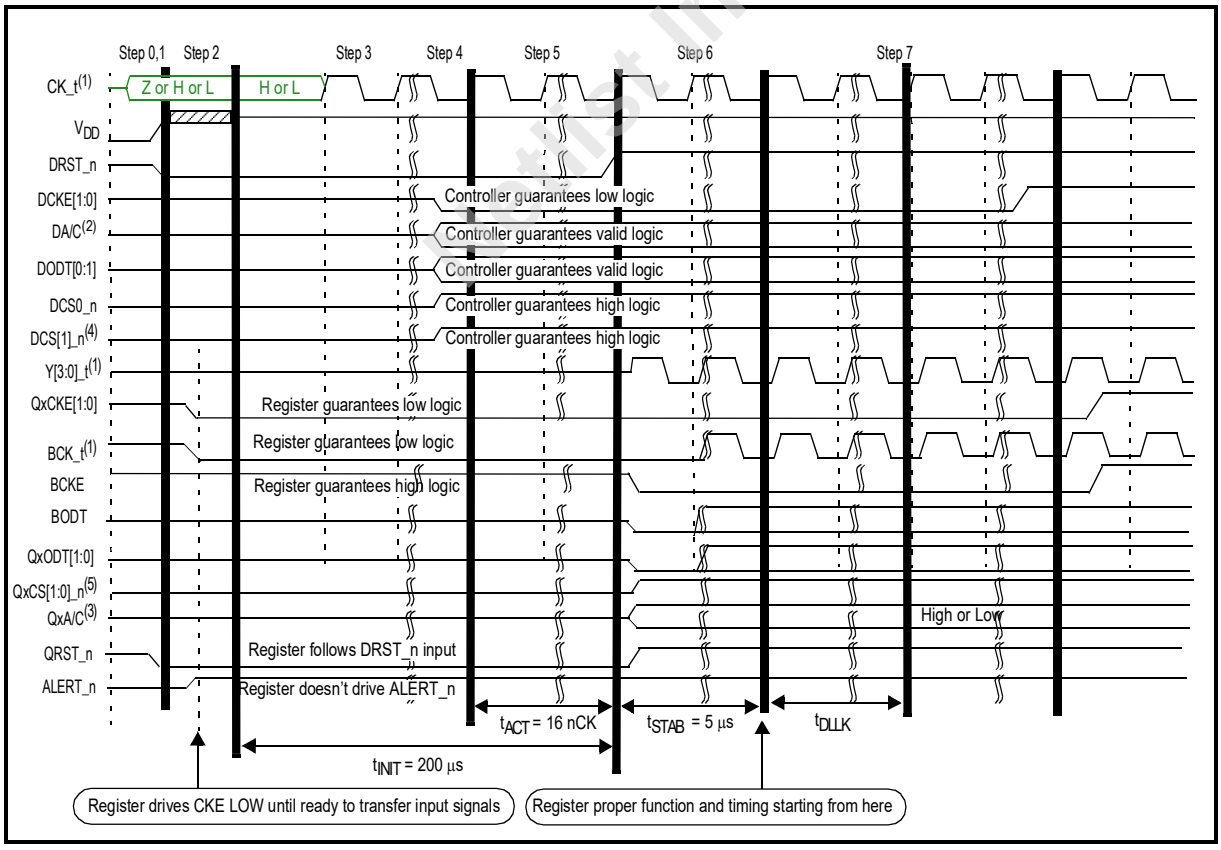

Figure 1 — Timing of clock and data during initialization sequence

1. CK_c,Y[3:0]_c and BCK_c left out for better visibility
2. DCKE0, DCKE1, DODT0, DODT1, DCS0_n and DCS1_n are not included in this range
3. QxCKEn, QxODTn, QxCSn_n are not included in this range.

4. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select inputs are present.
5. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select outputs (per side) are present.
6.) From step 6 onwards, the QxCS2_n and QxCS3_n outputs will initially be enabled and controlled directly by the DC0 and DC1 inputs, respectively, since Direct DualCS mode is enabled by default in F0RC0D. Therefore, it is required that the host always drives the DC0 and DC1 inputs with the correct levels needed for chip select signals during power on initialization for DIMMs utilizing QxCS2_n and QxCS3_n. This also applies in configurations using Encoded QuadCS mode.
7. The output pins QVrefCA and BVrefCA need to have valid $V_{DD}/2$ levels no later than at step 7.

From a device perspective, the initialization sequence must be as shown in Table 3.

Table 3 — DDR4RCD02 Device Initialization Sequence[1]

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
	V_{DD}, AV_{DD}, PV_{DD}	DRST_n	VrefCA	DCS[1:0]_n[2]	DODT0, DODT1	DCKE0, DCKE1	DA/C	DPAR	CK_t, CK_c	QxCS[1:0]_n[3]	QxODT0, QxODT1	QxCKE0, QxCKE1	QxA/C	ALERT_n	Y[3:0]_t, Y[3:0]_c
0	0V	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	Z	Z	Z	Z	Z	Z
1	0-->V_{DD}	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z
2	V_{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	X	Z	Z	L[4]	Z	H[4]	Z
3	V_{DD}	L	X or Z	X or Z	X or Z	X or Z	X or Z	X or Z	running	Z	Z	L	Z	H	Z
4	V_{DD}	L	X or Z	H	X or Z	L	X or Z	X or Z	running	Z	Z	L	Z	H	Z
5	V_{DD}	L	X or Z	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V_{DD}	H	X or Z	H	X	L	X	X	running	H	L[5]	L	X	H	running
7[6]	V_{DD}	H	X or Z	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 22, Table 23 and Table 24).					

1. X = Logic LOW or logic HIGH. Z = floating.
2. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select inputs are present.
3. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select outputs (per side) are present.
4. ALERT_n is pulled high externally and QxCKEn will be driven to this logic state by the register after DRST_n is driven LOW and V_{DD} is nominal.
5. This indicates the state of QxODTx after DRST_n switches from LOW-to-HIGH and before the rising CK_t edge (falling CK_c edge). After the first rising CK edge, within (t_{STAB} - t_{ACT}), the state of QxODTx is a function of DODTx (HIGH or LOW).
6. Step 7 is a typical usage example and is not a register requirement.

As part of the initialization all control words are reset to their default state which is "0". After initialization, the Host must write to those control registers whose contents are required for frequency and DIMM configuration.

2.3.1 Reset Initialization with Stable Power

The timing diagram in Figure 2 depicts the initialization sequence with stable power and clock. This will apply to the situation when we have a soft reset in the system. DRST_n will be asserted for minimum 1 µs. This DRST_n timing is based on DDR4 DRAM Reset Initialization with Stable Power requirement, and is a minimum requirement. Actual DRST_n timing can vary base on specific system requirement, but it cannot be less than 1 µs as required by JESD79-4. The outputs QACKE0, QACKE1, QBCKE0 and QBCKE1 and BCK_t/BCK_c must drive LOW and BCKE must drive HIGH during reset.

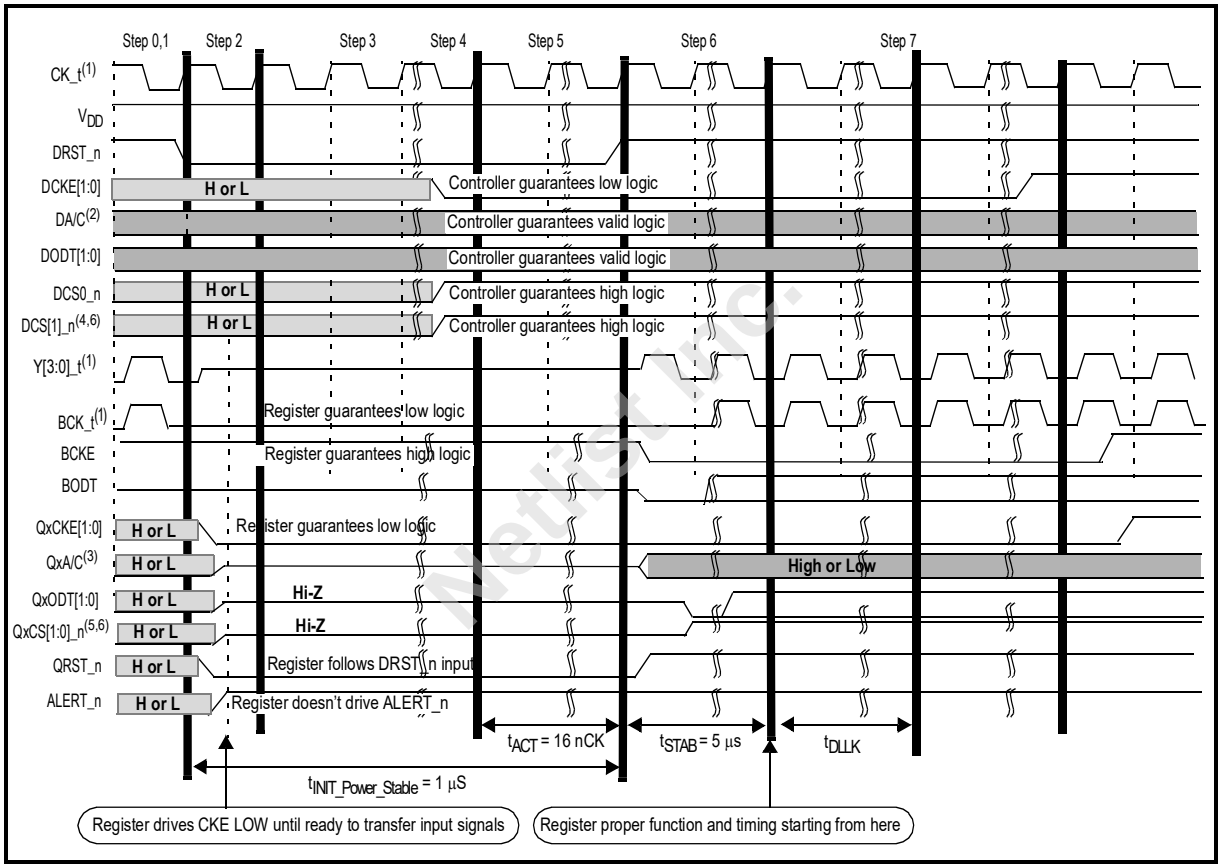

Figure 2 — Timing of clock and data during initialization sequence with stable power

1. CK_c,Y[3:0]_c and BCK_c left out for better visibility
2. DCKE0, DCKE1, DODT0, DODT1, DCS0_n and DCS1_n are not included in this range
3. QxCKEn, QxODTn, QxCSn_n are not included in this range.
4. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select inputs are present.
5. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select outputs (per side) are present.
6.) From step 6 onwards, the QxCS2_n and QxCS3_n outputs will initially be enabled and controlled directly by the DC0 and DC1 inputs, respectively, since Direct DualCS mode is enabled by default in F0RC0D. Therefore, it is required that the host always drives the DC0 and DC1 inputs with the correct levels needed for chip select signals during power on initialization for DIMMs utilizing QxCS2_n and QxCS3_n. This also applies in configurations using Encoded QuadCS mode.

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Table 4 — DDR4RCD02 Device Initialization Sequence[1] when Power and Clock are Stable

Step	Power	Inputs: Signals provided by the controller								Outputs: Signals provided by the device					
	V_{DD}, AV_{DD}, PV_{DD}	DRST_n	VrefCA	DCS[1:0]_n[2]	DODT0, DODT1	DCKE0, DCKE1	DA/C	DPAR	CK_t, CK_c	QCS[1:0]_n[3]	QxODT0, QxODT1	QxCKE0, QxCKE1	QxA/C	ALERT_n	Y[3:0]_t, Y[3:0]_c
0	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
1	V_{DD}	H	stable voltage	X	X	X	X	X	running	X	X	X	X	X	running
2	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L[4]	Z	H[4]	Z
3	V_{DD}	L	stable voltage	X	X	X	X	X	running	Z	Z	L	Z	H	Z
4	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
5	V_{DD}	L	stable voltage	H	X	L	X	X	running	Z	Z	L	Z	H	Z
6	V_{DD}	H	stable voltage	H	X	L	X	X	running	H	L[5]	L	X	H	running
7	V_{DD}	H	stable voltage	H	X	X	X	X	running	After Step 6 (Step 7 and beyond), the device outputs are as defined in the device Function Tables (see Table 22, Table 23 and Table 24).					

1. X = Logic LOW or logic HIGH. Z = floating.
2. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select inputs are present.
3. After DRST_n is driven LOW, Direct DualCS mode is selected in F0RC0D, i.e. only 2 chip select outputs (per side) are present.
4. ALERT_n is pulled high externally and QxCKEn will be driven to this logic state by the register after DRST_n is driven LOW and V_{DD} is nominal.
5. This indicates the state of QxODTx after DRST_n switches from LOW-to-HIGH and before the rising CK_t edge (falling CK_c edge). After the first rising CK edge, within (t_{STAB} - t_{ACT}), the state of QxODTx is a function of DODTx (HIGH or LOW).

2.4 Parity

The DDR4RCD02 includes a parity checking function. The DDR4RCD02 accepts a parity bit at its input pin DPAR one cycle after the corresponding data input.

If parity checking is enabled, the register only forwards sampled commands to the outputs when no parity error occurred. Since comparing the incoming parity against the parity calculated from the data received one cycle earlier requires a small logic delay, a programmable command latency[1] is available in the Command Latency Adder control word F0RC0F. The min CLA setting with parity enabled is 1 tCK. The latency from DCA input to QCA output is always one cycle greater than the latency from DPAR to QxPAR. Since the DDR4 DRAMs expect the parity input in the same cycle as data, the QxPAR outputs (if enabled) are always sent in the same cycle as the corresponding data outputs. It is the responsibility of the host to ensure Parity control word and the Command Latency Adder control word are programmed in a compatible way.

If parity checking is disabled, the register forwards sampled commands to the outputs unconditionally, i.e. the

1. The definition of 'Command' in this context also includes the QxCSy_n, QxCKEn and QxODTn signals.

command appears on the outputs regardless of whether a parity error occurred or not.

The output timing is determined by the Command Latency Adder control word regardless of whether the device has parity checking enabled or disabled. The behavior with parity checking disabled is the same with the exception that ALERT_n is never asserted as result of a CA parity error (but can still be asserted as a result of an assertion of the ERROR_IN_n input). Even with parity checking disabled the DPAR input is forwarded to both QxPAR outputs (if they are enabled), which are asserted in the same cycle as the command output.

After the DDR4RCD02 receives DPAR from the memory controller, it compares it with the data received on the CA inputs and indicates on its open-drain ALERT_n pin (active LOW) whether a parity error has occurred. The computation only takes place for data which is qualified by at least one of the DCS[n:0]_n signals being LOW.

The convention of parity is even parity, i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even. The DIMM-dependent control signals (DCKE0, DCKE1, DCS0_n .. DCS3_n, DODT0 and DODT1) are not included in the parity check computations.

Even after a CA parity error has been registered, the device will still forward DCKEn and DODTn to the DRAMs, and the device will enter CKE power down mode depending on the DCKEn transitions.

If a parity error occurs and parity checking is enabled in F0RC0E, the DDR4 register sets the 'CA Parity Error Status' bit in F0RCFx to '1'and disables parity checking. ALERT_n is asserted three input clocks after the erroneous command is registered. If Control Gear-down mode is enabled, ALERT_n will be asserted on an even and fixed number of clock cycles after the erroneous command is registered. The assertion of the ALERT_n will either be after four cycles or after six cycles depending on the implementation of Control Gear-down in the RCD. If the 'CA Parity Error Status' bit is '0', the DDR4 register logs the error by storing the erroneous command and address bits in the Error Log Register. ALERT_n stays asserted LOW until a 'Clear CA Parity Error Status' command is sent if the 'ALERT_n Assertion' bit in the Parity Control Word (F0RC0E) is '0'. In this case the erroneous command and all subsequent commands are not forwarded[1] (i.e. QxCSy_n are not asserted) to the DRAM until the memory controller issues a 'Clear CA Parity Error' command, which will also clear the 'CA Parity Error Status' bit in the Error Log Register. If the 'ALERT_n Assertion' bit is '1', the ALERT_n pulse width is as defined in Table 47 with start of the ALERT_n pulse width counted from the third input clock edge after the 1st parity error. If the 'ALERT_n Re-enable' bit is '0', the erroneous command and all subsequent commands are not forwarded (i.e. QxCSy_n are not asserted) to the DRAM until the end of the ALERT_n pulse width and parity checking remains disabled until a 'Clear CA Parity Error' command is sent, which will also clear the 'CA Parity Error Status' bit in the Error Log Register. If the 'ALERT_n Re-enable' bit is '1', the device will re-enable parity after the ALERT_n pulse and the device will forward commands to the DRAM. The 'CA Parity Error Status' bit will remain set. If a subsequent parity error is detected, the device will re-enter the parity error state and set the '> 1 Error' bit. The other bits in the Error Log Register are not updated on this subsequent error. Both the 'CA Parity Error Status' bit as well as the '> 1 Error' bit will be cleared by sending a 'Clear CA Parity Error' command.

Using the CW Source Selection & CW Destination Selection control words (See "CW Selection Control Words" on page 85.) and CW Data control word (See "F0RC6x: CW Data Control Word" on page 86.), the host can read the Error Log Register by writing it first into page 0 of the DRAM MPR, from where the host can read it using the defined DDR4 DRAM MPR read functionality.

2.4.1 Parity Timing Scheme Waveforms

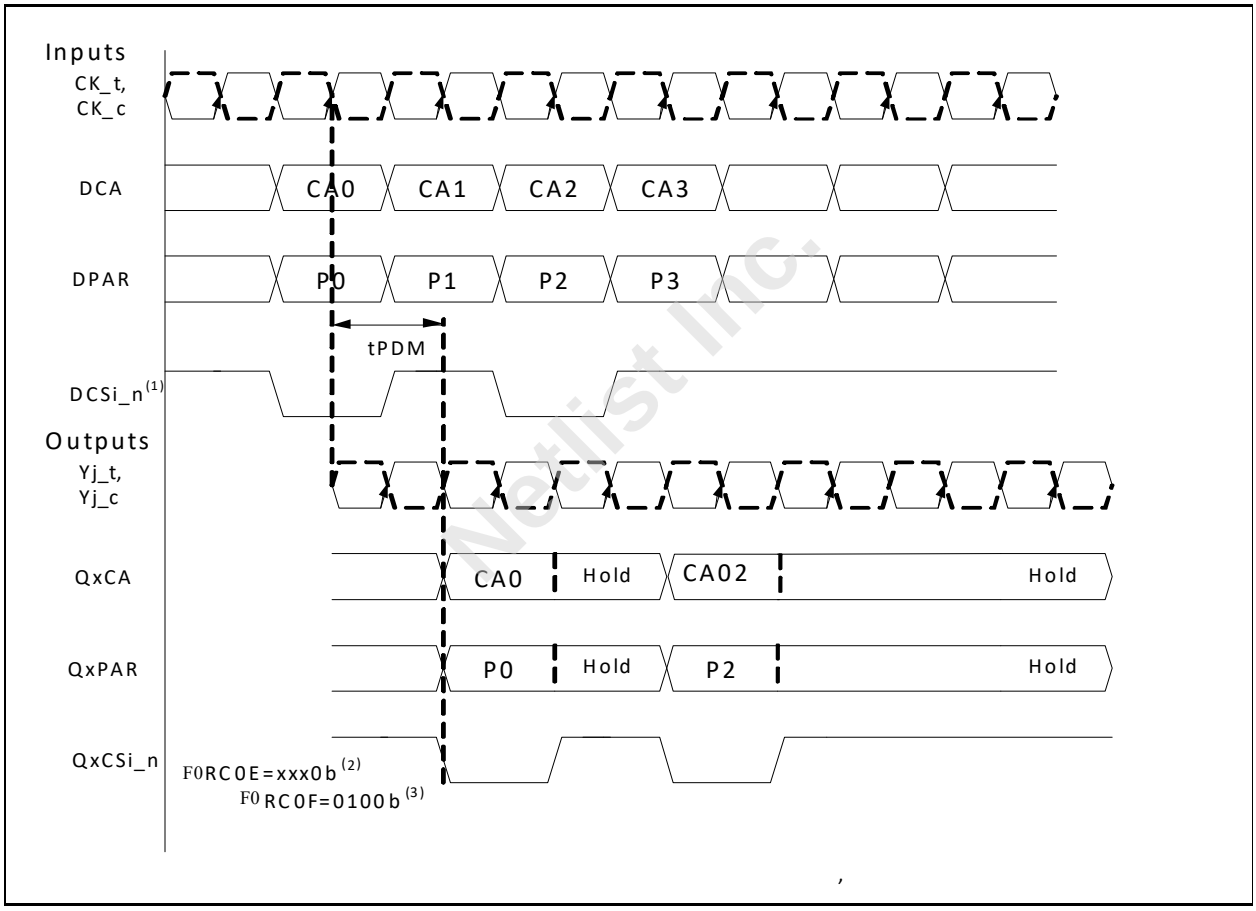
In Figure 5 and Figure 6 both the clock, data and parity input signals as well as the associated output signals are shown to illustrate the effect of the programmable command latency control bits. All other timing diagrams depict

1. However, CMD4 MPR writes to the DRAM that are the result of 'CW Write' commands to F0RC06 are still allowed.

only the input signals and the ALERT_n output.

The DPAR signal arrives one input clock cycle after the corresponding data input signals. ALERT_n is asserted three input clock cycles after the corresponding data is registered. If Parity is enabled and the ALERT_n assertion bit in the **Parity , NV Mode Enable, and ALERT Configuration** Control Word is set, ALERT_n will stay LOW for a minimum of 'minimum ALERT_n pulse width' (see Table 47) clock cycles or until DRST_n is driven LOW. If Parity is enabled and the ALERT_n assertion bit in the **Parity , NV Mode Enable, and ALERT Configuration** Control Word is cleared, ALERT_n will be deasserted when a 'Clear CA Parity Error' command is received or when DRST_n is driven LOW.

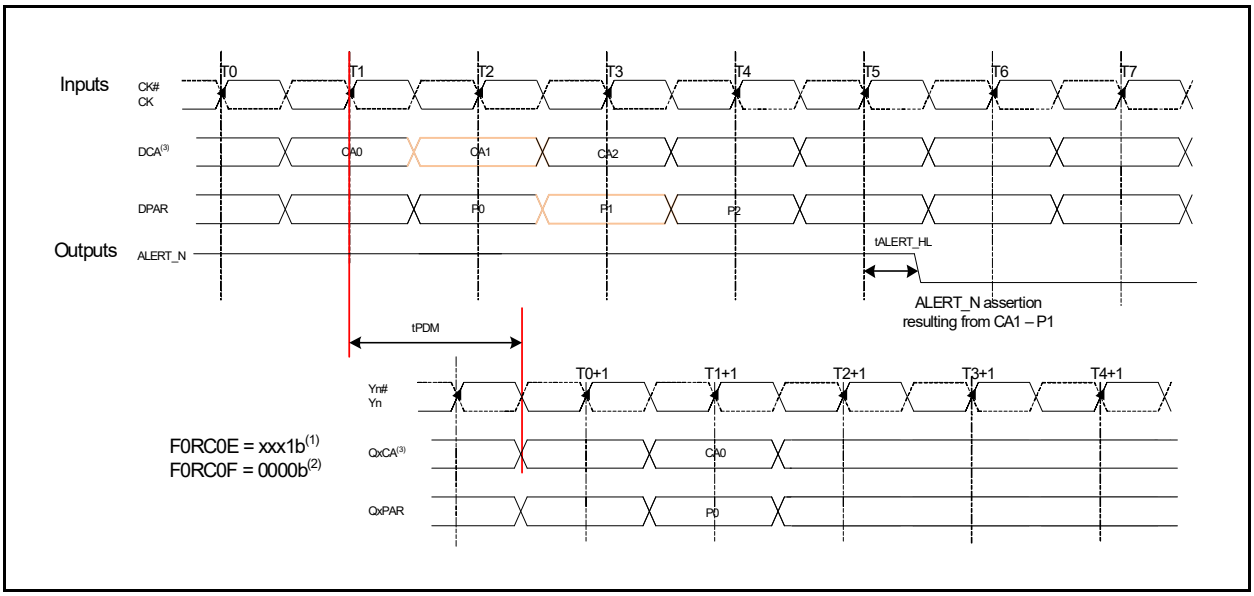
Figure 3 shows the timing diagram with an additional command latency of 0 which requires parity checking to be disabled.



(1) Assuming only one rank selected, all other DCSx_n are high
(2) Parity checking is disabled
(3) Additional Command latency = 0

Figure 3 — Timing of clock, data and parity signals with parity checking disabled

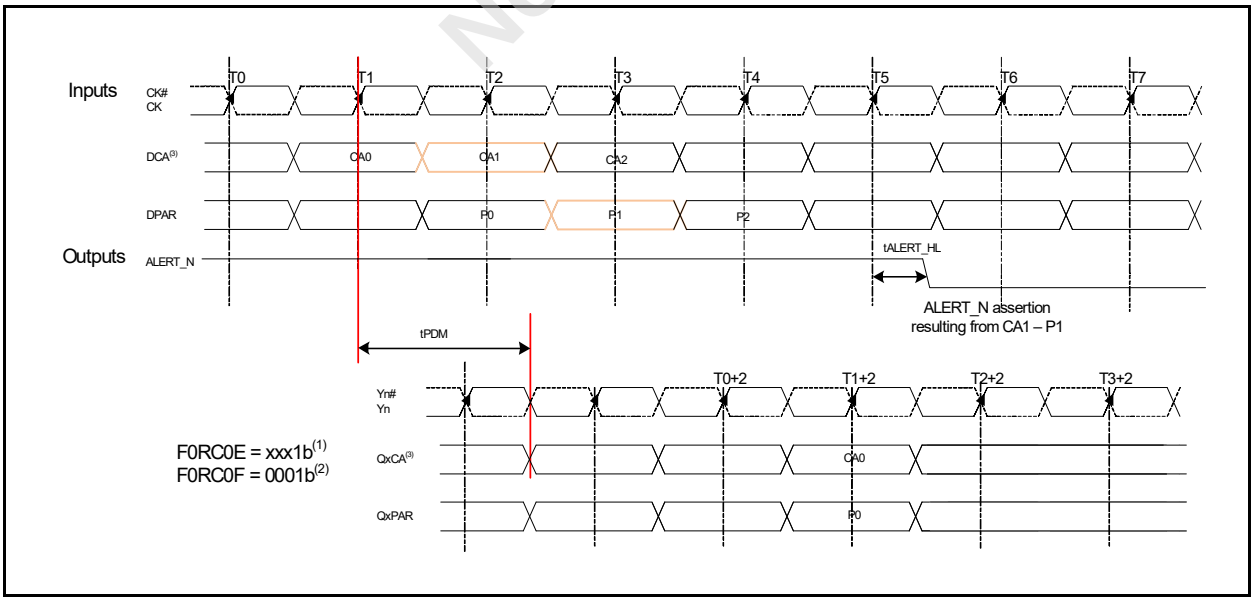
Figure 4 shows the parity diagram with single parity-error occurrence with an additional command latency of 1 and assumes the occurrence of only one parity error when data is clocked in at the T2 input clock cycle (DPAR clocked in on the T3 input clock cycle).



(1) Parity checking is enabled
(2) Additional Command latency = 1
(3) Each command CAx is accompanied by a DCSx_n or QxCSy_n assertion which is not shown for better visibility

Figure 4 — Timing of clock, data and parity signals with checking enabled and latency=1

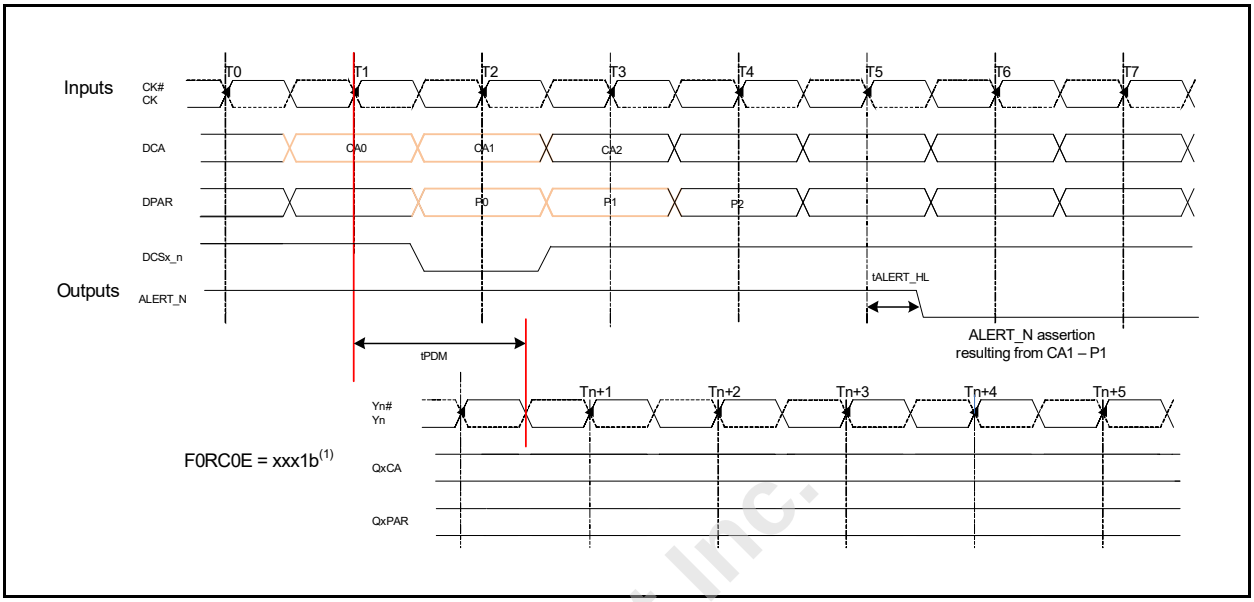
Figure 5 shows the parity diagram with single parity-error occurrence with an additional command latency of 2 and assumes the occurrence of only one parity error when data is clocked in at the T2 input clock cycle (DPAR clocked in on the T3 input clock cycle).



(1) Parity checking is enabled
(2) Additional Command latency = 2
(3) Each command CAx is accompanied by a DCSx_n or QxCSy_n assertion which is not shown for better visibility

Figure 5 — Timing of clock, data and parity signals with checking enabled and latency=2

Figure 6 shows the parity diagram with two parity-error occurrences; during chip-deselect and chip-select modes. The diagram assumes the occurrence of both parity errors when data is clocked in at the T1 and T2 input clock cycles (DPAR clocked in on the T2 and T3 input clock cycles). Parity error in the chip-deselect mode is ignored, but parity error in the chip-select mode is detected.



(1) Parity checking is enabled

Figure 6 — Parity-error occurrence on chip-deselect mode

2.5 Data Buffer Control Bus

This section describes the signals used in the DDR4 LRDIMM control bus that connects the DDR4 Register with each of the nine DDR4 data buffers (DB). This interface is enabled on power-on and only disabled when the 'LRDIMM Disable' bit in the DIMM Configuration Control Word (F0RC0D) is set.

2.5.1 Control Bus Signals

Table 5 — List of Signals for Data Buffer control

Name	Description	Signal Count
BCOM[3:0]	Data buffer command signals	4
BCKE	Function of registered DCKE (dedicated non-encoded signal)	1
BODT	Function of registered DODT (dedicated non-encoded signal)	1
BCK_t, BCK_c	Clock outputs for the data buffers	2
BVrefCA	Reference voltage output for command and control signals connected to the data buffers	1
	Total	9

2.5.2 Control Bus Timing

The output signals BCOM, BODT and BCKE are driven at the same time as the QxCA outputs, i.e. they are affected by the Command Latency Adder Control Word F0RC0F but a latency adder of 0 is not a valid configuration.

2.5.3 Control Bus Commands

2.5.3.1 Command List

Table 6 — Data Buffer Control Bus Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information for regular reads or MPR number for MPR override reads in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU[1]	Reserved for future use	1110
RFU[1]	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

2.5.3.2 Command Sequences

With the exception of the NOP command, all commands require more than one clock cycle in order to send additional information needed by the buffer in the execution of the command. We call this succession of command and its corresponding data transfers a command sequence. The command sequence for Read or Write commands requires two additional cycles to transfer the rank number corresponding to the write or read command, the sequence for MRS Writes requires seven clock cycles in addition to the basic command, the sequence for the BCW Write command uses six additional clock cycles and the BCW Read command uses five additional clock cycles.

2.5.3.3 Parity Error Checking

Command sequences are protected by a parity checking scheme. Parity checking on the command bus signals is disabled by default, and it is necessary to enable parity checking by writing a buffer configuration bit by using a BCW instruction. The DDR4RCD02 always generates the parity cycles in the BCOM command sequences. Parity checking only applies to the BCOM[3:0] signals. The convention of parity is even parity, i.e. valid parity is defined as

an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even. Parity will be checked in accumulated sequential fashion during all the cycles of a command sequence. The parity bit is transmitted for each BCOM[3:0] signal in the corresponding BCOM[3:0] line during the last transfer (clock cycle) in the command sequence.

2.5.3.4 Command Sequence Error Detection

In order to keep the command bus from getting stuck in an out-of-sync situation in terms of the handling of command versus data transfers, a protection scheme is necessary.

Details of the command sequence error detection algorithm are documented in the DDR4 DB specification.

Upon detection of a command sequence error, the DB will assert its ALERT_n output which is assumed to be routed to the ERROR_IN_n input of the RCD, where it causes the assertion of the RCD ALERT_n output.

The RCD will not change its operation in response to the input signal level at the ERROR_IN_n input.

2.5.3.5 Error Handling

The error handler in the host will use the length of the RCD's ALERT_n output pulse to determine what kind of error occurred and if necessary read the error log register of the RCD as well as the error log register of the DDR4 DRAMs and data buffers to determine the source of the error and the specific command that caused the error.

The host may or may not try to recover from the error condition by retrying the affected commands.

2.5.4 Command Sequence Descriptions

The timing diagrams in this section show only the lower nibble of the DDR4RCD02. The same timing relationships apply independently also for the upper nibble. The timing diagrams only show the case of burst length = 8 and preamble = 1 nCK but equivalent timing relationships exist for burst length = 4 & 10 and preamble = 2 nCK.

For readability reasons, the timing diagrams use the abbreviations DB_RL and DB_WL for the latency between first cycle of RD command and the first rising edge of MDQS at DDR4DB02 inputs and for the latency between first cycle of WR command and the first rising edge of MDQS at DDR4DB02 outputs respectively. Both DB_RL and DB_WL include full cycle and fractional cycle delays. The equations for these latencies are as follows:

$DB\_WL(R)^1 = CWL + AL + PL + DWL(R)$

$DB\_RL(R)^2 = CL + AL + PL + MRE(R) + tRPRE/2$

tRPRE/2 exists in DB_RL since the host will adjust the receive enable delay MRE(R) to place it in the center of the read preamble.

For the detailed equations for DWL and MRE refer to the DDR4DB02 specification.

The DDR4RCD02 delays tPDM_RD and tPDM_WR are defined as the delay between first rising edge of MDQS and the first rising edge of DQS for a RD command and as the delay between first rising edge of DQS and the first rising edge of MDQS for a WR command respectively. By default these delays are constant per DDR4RCD02 for all ranks and nibbles.

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1. This equation assumes that the DDR4 data buffer MDQ-MDQS Write Delay Control Words in F[3:0]BC8x/ F[3:0]BC9x are at their default power-on setting.
2. This equation assumes that the DDR4 data buffer MDQS Read Delay Control Words in F[3:0]BC4x/ F[3:0]BC5x are at their default power-on setting.

Timing parameters that are integer multiples of tCK are shown in **bold blue** letters while timing parameters that are analog non-integer multiples or fractions of tCK are shown in *red italic* letters.

For simplicity the timing diagrams only show one of the possible host interface termination modes and RTT_PARK is never shown even though it is always supported.

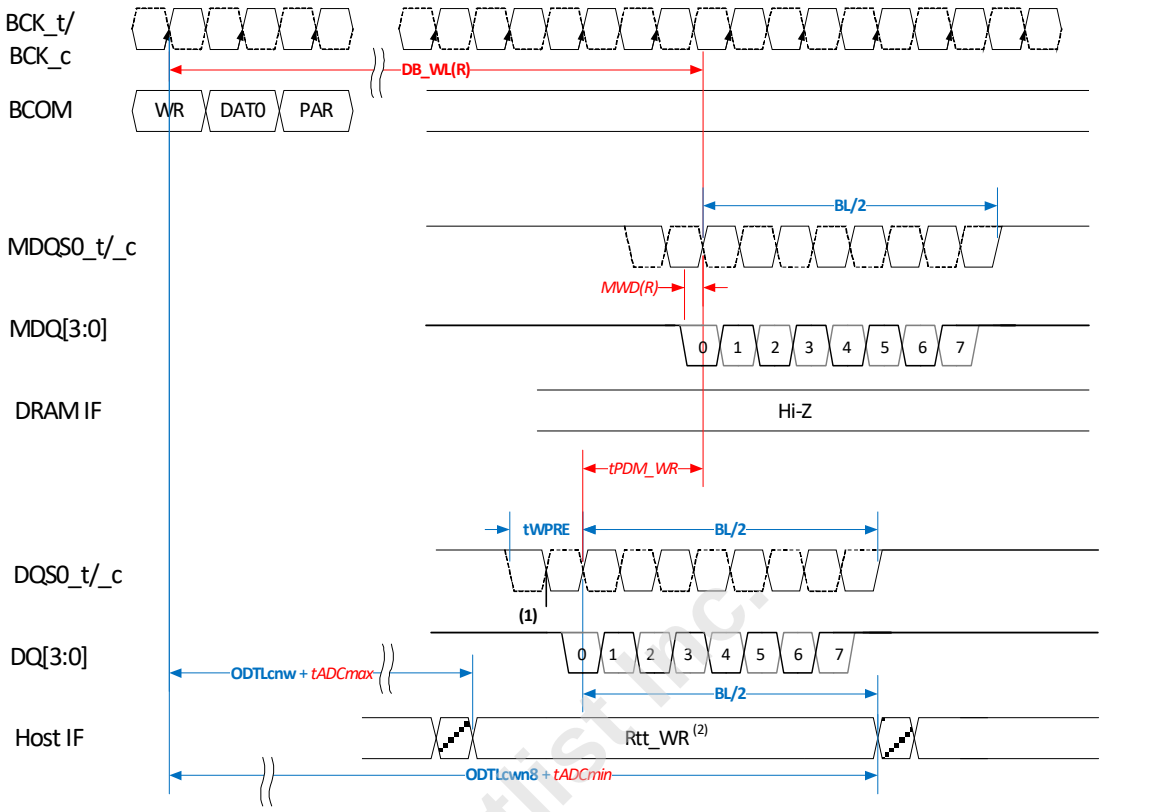
2.5.4.1 Write Commands

Table 7 shows the sequence for write (WR4, WR8) commands. Each write command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. If CRC is enabled in the DRAM and in the DB (F4BC2x, DA7), the burst length will always be 10UI.

Table 7 — Multicycle Sequence for Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	WR	Write command BCOM[3:0] = 1000
2	DAT0	Transfer the rank ID for write command BCOM[1:0] = {RANK_ID[1:0]} for DRAM writes Burst length information for Write data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for WR command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

Figure 7 shows the timing sequence for a Write command.



(1) Host Interface Receivers turn-on in the middle of the pre-amble. If DDR4DB02 DFE feature is enabled Receivers may turn-on earlier.
(2) If Dynamic ODT is enabled in BC01

Figure 7 — WRITE Timing

2.5.4.2 Read Commands and MPR Override Reads

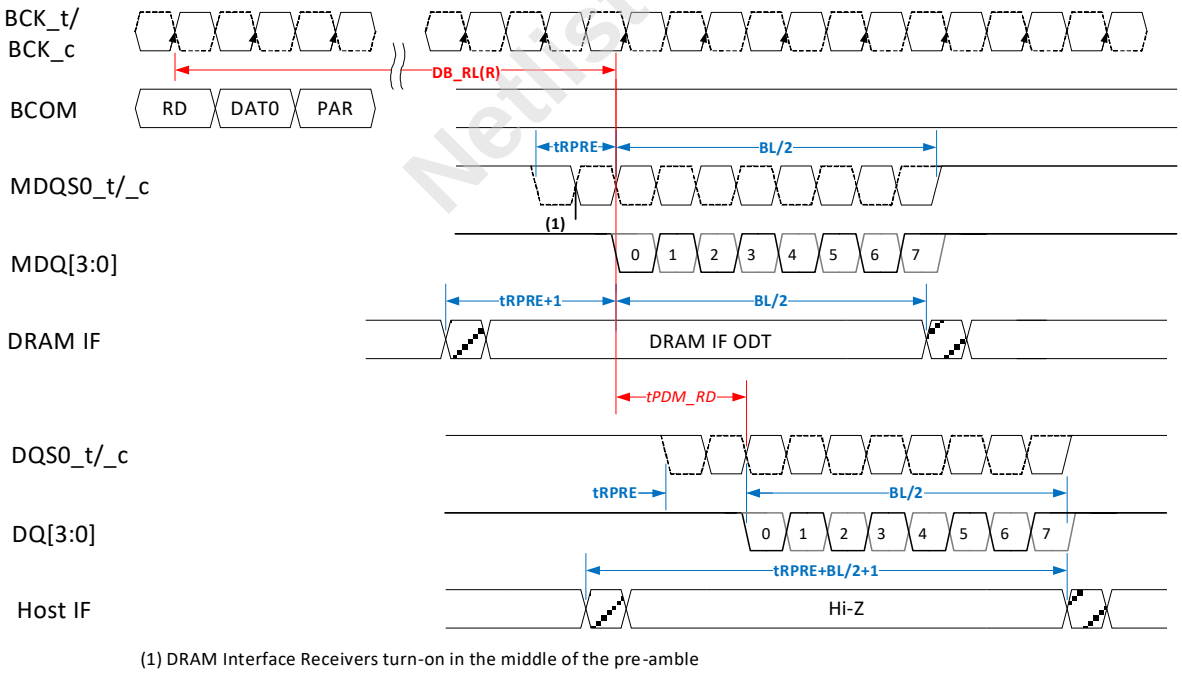
Table 8 shows the sequence for read (RD4, RD8) commands. Each read command is followed by a one-cycle transfer that contains the rank ID that selects 1 rank out of 4 that needs to be accessed and the burst length information for the data transfer and the parity bits in the last transfer cycle. The rank ID may be used to make rank-specific adjustments to the timing controls if necessary. The BCOM[2] bit in DAT0 is only valid for on-the-fly burst length. This bit is ignored by the DB if the BL field in the MR0 snoop register is set for fixed burst length of 8 or 4 (A[1:0] = '00' or '10')

.

Table 8 — Multicycle Sequence for Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	RD	Read command BCOM[3:0] = 1001
2	DAT0	Transfer the rank ID for read command or the MPR selection ID in MPR override read mode BCOM[1:0] = {RANK_ID[1:0]} for DRAM reads BCOM[1:0] = {BA1, BA0} for MPR override reads Burst length information for Read data BCOM[3:2] = {0, 0} for BC4 BCOM[3:2] = {0, 1} for BC8
3	PAR[3:0]	Even parity bits for RD command and data PAR[x]: Parity bit for previous two BCOM[x] transfers
4	Next Cmd	Next Command

Figure 8 shows the timing sequence for a Read command.



(1) DRAM Interface Receivers turn-on in the middle of the pre-amble

Figure 8 — READ Timing

Read commands can be used to access locations other than the memory array in the DDR4 DRAM devices. These special read commands are MPR override reads which access the MPR locations inside the DB. MPR override mode is configured in the DB. Since there is only one set of MPR registers in the DB, the RCD ignores the rank information

when it sends the Read command to the DB and sends the BA[1:0] bits (indicating which of the three MPR locations are accessed) instead of the rank information in the first data cycle. MPR override reads are only allowed to rank 0, i.e. the RCD never mirrors BA0 and BA1 for MPR override reads.

2.5.4.3 MRS Write Commands

The DDR4RCD02 generates MRS Write commands to the data buffers for each MRS command to the A-side DRAMs (i.e. with BG1 = 0) for rank 0 only. The register does not generate MRS Write commands to the data buffer for MRS commands to the B-side DRAMs (i.e. with BG1='1') or for MSR commands ranks other than 0.

Table 9 shows the sequence for MRS Write commands.

Table 9 — Multicycle Sequence for MRS Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	MRS Write	MRS Write Command BCOM[3:0] = 1011
2	DAT0	MRS ID code BCOM[3:0] = {0, BG0, BA1, BA0}
3	DAT1	First data transfer for MRS Write command BCOM[3:0] = {0, DA2, DA1, DA0]
4	DAT2	Second data transfer for MRS Write command BCOM[3:0] = {0, DA5, DA4, DA3}
5	DAT3	Third data transfer for MRS Write command BCOM[3:0] = {0, DA8, DA7, DA6}
6	DAT4	Fourth data transfer for MRS Write command BCOM[3:0] = {0, DA11, DA10, DA9}
7	DAT5	Fifth data transfer for MRS Write command BCOM[3:0] = {0, 0, DA13, DA12}
8	PAR[3:0]	Even parity bits for MRS Write command and data PAR[x]: parity bit for 7 previous BCOM[x] transfers
9	Next Cmd	Next Command

The sequence for an MRS Write command is shown in Figure 9 below. The timing diagrams show how the MRS Write command is followed by six data transfer cycles and a parity data transfer cycle. Since the command sequence uses eight cycles it is necessary to include these cycles as part of the tBCW parameter that indicates the spacing from the MRS Write command to the following valid command (also shown in the diagrams). The number of additional transfers on the BCOM bus after the MRS Write command also imposes a limitation on how close consecutive MRS Write commands can be issued to the data buffer.

For MRS Write commands in PDA (Per DRAM Addressability) mode when the DIMM type bit in F0RC0D is set to '0' (LRDIMM), the DDR4RCD02 generates a BCOM Write command instead of a BCOM MRS Write command in order to forward the data buffer's host interface DQ inputs to the DRAMs which use their DQ0 pins for device selection. The DB will not capture any MRS bits written in PDA mode.

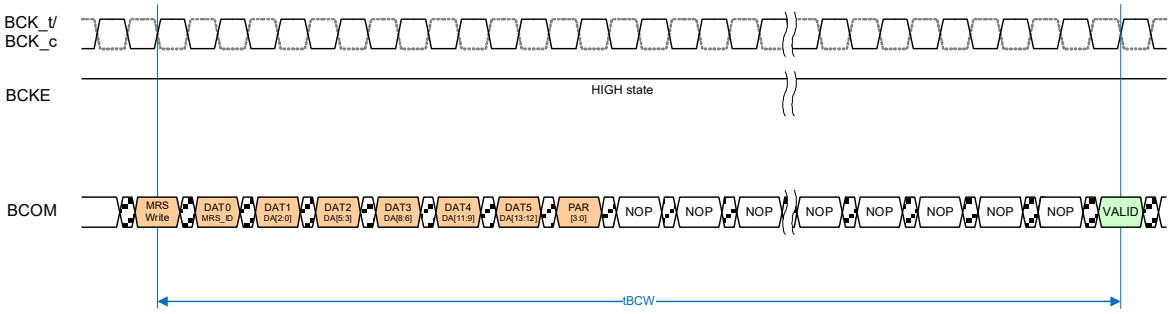


Figure 9 — MRS Write command sequence

2.5.4.4 BCW Write Command

Table 10 shows the sequence for buffer control word write commands.

Table 10 — Multicycle Sequence for BCW Write Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Write	Buffer control word write access command BCOM[3:0] = 1100
2	DAT0	First data transfer for BCW Write command BCOM[3:0] = {0, DA2, DA1, DA0]
3	DAT1	Second data transfer for BCW Write command BCOM[3:0] = {0, DA5, DA4, DA3}
4	DAT2	Third data transfer for BCW Write command BCOM[3:0] = {0, DA8, DA7, DA6}
5	DAT3	Fourth data transfer for BCW Write command BCOM[3:0] = {0, DA11, DA10, DA9}
6	DAT4	Fifth data transfer for BCW Write command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW writes BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW writes BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW writes BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW writes BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW writes BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW writes BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW writes BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW writes
7	PAR[3:0]	Even parity bits for BCW Write command and data PAR[x]: parity bit for 6 previous BCOM[x] transfers
8	Next Cmd	Next Command

The sequence for a BCW Write command is shown in Figure 10 below. The timing diagrams show how the BCW Write command is followed by five data transfer cycles and a parity data transfer cycle. Since the command sequence uses seven cycles it is necessary to include these cycles as part of the tMRD parameter that indicates the spacing from the BCW Write command to the following valid command (also shown in the diagrams).

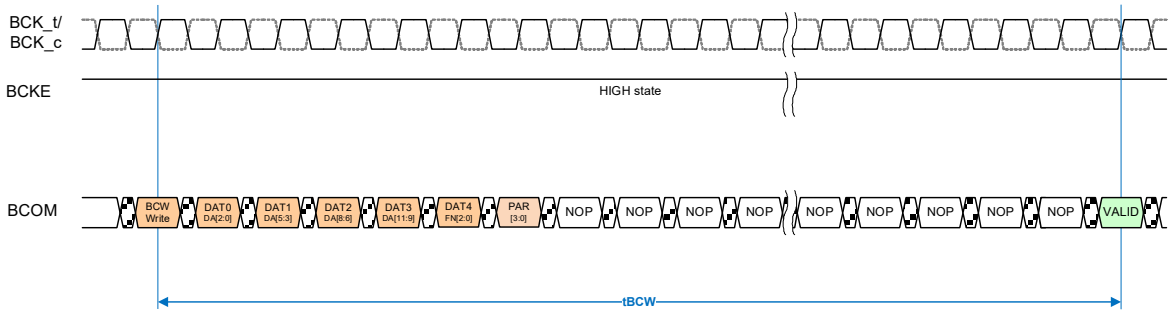


Figure 10 — Buffer Control Word Write command sequence

2.5.4.5 BCW Read Commands

The DDR4RCD02 generates a BCW Read command on the buffer control bus when it receives a CW Read command in F0RC06 with A12 = 1.

Table 11 shows the sequence for BCW Read commands.

Table 11 — Multicycle Sequence for BCW Read Commands

Time (clock cycle)	BCOM[3:0]	Description
0	Prev Cmd	Previous command or data transfer
1	BCW Read	Buffer control word read access command BCOM[3:0] = 1101
2	DAT0	First data transfer for BCW Read command BCOM[3:0] = {0, DA5, DA4, 0}
3	DAT1	Second data transfer for BCW Read command BCOM[3:0] = {0, DA8, DA7, DA6}
4	DAT2	Third data transfer for BCW Read command BCOM[3:0] = {0, DA11, DA10, DA9}
5	DAT3	Fourth data transfer for BCW Read command BCOM[3:0] = {0, 0, 0, 0} for Function space 0 BCW reads BCOM[3:0] = {0, 0, 0, 1} for Function space 1 BCW reads BCOM[3:0] = {0, 0, 1, 0} for Function space 2 BCW reads BCOM[3:0] = {0, 0, 1, 1} for Function space 3 BCW reads BCOM[3:0] = {0, 1, 0, 0} for Function space 4 BCW reads BCOM[3:0] = {0, 1, 0, 1} for Function space 5 BCW reads BCOM[3:0] = {0, 1, 1, 0} for Function space 6 BCW reads BCOM[3:0] = {0, 1, 1, 1} for Function space 7 BCW reads
6	PAR[3:0]	Even parity bits for BCW Read command and data PAR[x]: parity bit for 5 previous BCOM[x] transfers
7	Next Cmd	Next Command

The sequence for BCW Read command is shown in Figure 11 below. The timing diagrams show how the BCW Read command is followed by four data transfer cycles and a parity data transfer cycle. This BCW Read command moves the selected BCW bits to MPR0 and configures the DB for MPR override read mode for the next Read command. The DB treats the first Read command after a BCW Read command as an MPR0 override read (regardless of the BCOM[1:0] bits during the DAT0 cycle of the corresponding BCOM Read command). The read data is driven out after DB_RL(R0) on the host interface DQ pins after the Read command. Just like in regular MPR override read mode, DDR4RCD02 will forward Read command to DRAM but DDR4DB02 will ignore read data from DRAM.

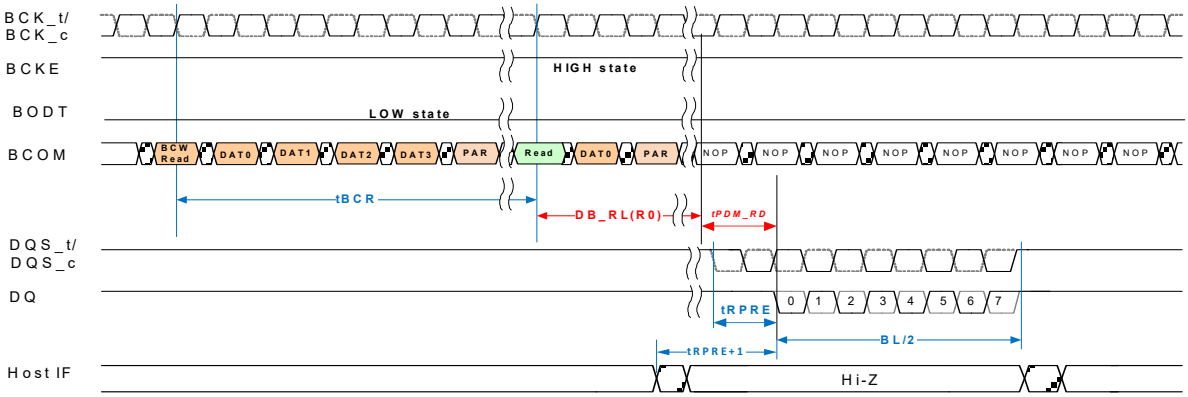


Figure 11 — BCW Read command sequence

2.6 DQ Bus Termination in LRDIMM application

The DDR4RCD02 supports DQ bus termination in LRDIMM applications (i.e. with data buffers connected to it) by providing the BODT output connected to the data buffers.

Unless BODT is turned off in F0RC8x bits DA[5] or DA[7], BODT is the logical OR of the DODT0 and DODT1 inputs, i.e. if one or both of these inputs is asserted HIGH, the BODT output is asserted HIGH.

When BODT is enabled, the host controls enabling RTT_NOM on the host interface of the data buffer through assertion of the DODT signals, which are OR'ed by the RCD, which in turn asserts BODT HIGH or LOW to the data buffer. The enabling/disabling of the on-die termination at the DRAM interface of the data buffer is independent from the BODT input control signal.

The timing for enabling RTT_NOM on the host interface in response to BODT being captured HIGH is dependent on the DRAM interface write leveling control words in a similar way as the host interface receive enable timing during data transactions resulting from WRITE commands is dependent on the DRAM interface write leveling control words. The data buffer hardware applies a fixed fall-through delay from the trained DRAM interface write timing back to the host interface termination enable timing. The host interface termination enable timing has two or three cycles less of latency with respect to the BODT signal assertion than the latency for enabling the host interface DQS_t/DQS_c receivers after a WRITE command is received, depending on the length of the write preamble.

It is the responsibility of the host to assert the DODT signal to the RCD early enough to ensure that the host interface termination is active prior to start of the read preamble at the host interface. The duration of the data buffer's RTT_NOM termination is controlled by the host through the length of the DODT pulse.

Since the data buffer can either drive data or terminate (but not both at the same time), the data buffer disables RTT_NOM at the host interface for reads targeted to this DIMM during the duration of the read burst (including the Read Preamble).

The timing for enabling RTT_WR on the host interface in response to a WRITE command being captured on the BCOM inputs is dependent on the DRAM interface write leveling control words in a similar way as the host interface receive enable timing during data transactions resulting from WRITE commands is dependent on the DRAM interface write leveling control words. The data buffer hardware applies a fixed fall-through delay from the trained DRAM interface write timing back to the host interface termination enable timing. The host interface termination enable timing has two or three cycles less of latency with respect to the WRITE command capture than the latency for enabling the host interface DQS_t/DQS_c receivers after a WRITE command is received, depending on the length of the write preamble.

Figure 12 shows the host interface ODT timing based on the assertion of the input signal BODT. The DDR4DB02 parameters ODTLon, ODTLoff, ODTLcnw, ODTLcwn and tADC are defined in the Electrical and Timing chapter of the Data Buffer Specification. For simplicity this diagram shows ODT timings always aligned with rising clock edges but due to the existence of the fractional cycle delays DB_WL(R) and tPDM_WR or tPDM_WR_RA, this is typically not the case.

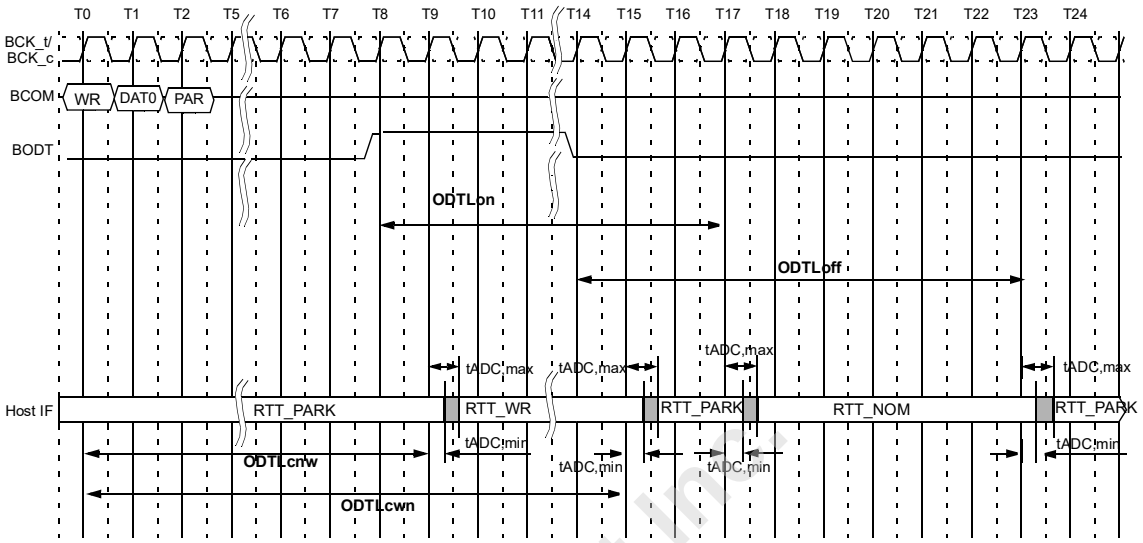


Figure 12 — BODT timing (Dynamic ODT, 1tCK preamble, CL=14, CWL=11, BL=8, AL=0, CRC Disabled)

DB_WL(R) = CWL + AL + PL + DWL(R)

ODTLon = DB_WL(R[1]) - tPDM_WR - tWPRE -1; where tWPRE = 1 or 2 (when F0BC1x DA7 = 0)

= DB_WL(R[1]) - tPDM_WR_RA - tWPRE -1; where tWPRE = 1 or 2 (when F0BC1x DA7 = 1)

ODTLoff = ODTLon

ODTLcnw = DB_WL(R) - tPDM_WR - tWPRE -1; where tWPRE = 1 or 2 (when F0BC1x DA7 = 0)

= DB_WL(R) - tPDM_WR_RA - tWPRE -1; where tWPRE = 1 or 2 (when F0BC1x DA7 = 1)

ODTLcwn = ODTLcnw + tWPRE + BL/2 +1; where tWPRE = 1 or 2 and BL = 4, 8 or 10 with CRC enabled

Unless F0RC8x bit DA[7] = 1, the host also controls the QxODT signals at the DRAM interface directly through the assertion of the two DODT signals at the host interface. The host may utilize non-target termination to a rank on the same DIMM other than the target rank for read transactions. The host may also utilize non-target termination to a rank on the same DIMM other than the target rank for write transactions.

If F0RC8x DA[7:6] = 11, the assertion of the QxODT outputs is caused by the capture of a Write or Read command, controlled by the rules in F0RC9x and F0RCAx respectively. The assertion timing of the QxODT pulse is controlled by F0RC8x bits DA[4:0] and F0RC5x bits DA[3:0]. Table 12 shows the default QxODT[1:0] high times for Write

1. RTT_NOM termination without a coinciding DDR4DB02 data movement (e.g. WR) uses rank 0 timing while RTT_NOM termination with a coinciding data movement will use the timing of the target rank, which implies that the data buffer can dynamically switch between different rank timings from one access to the next.

and Read commands.

Table 12 — Default Write, Read QxODT[1:0][1] Signal High Time

Operation	Pre-amble	Burst Length	QxODT[1:0] High Time		Unit
			Write CRC Disabled	Write CRC Enabled	
Write	1 nCK	BL8	6	7	nCK
		BC4	4	7	
	2 nCK	BL8	7	8	
		BC4	5	8	
Read	1 nCK	BL8	6		
		BC4	4		
	2 nCK	BL8	7		
		BC4	5		

1. Only applicable if F0RC8x DA[7:6] = 11. Applies to QxODT[1:0] Write and Read patterns that are selected in F0RC9x and RCAx respectively. The DDR4RCD02 is responsible for monitoring DRAM MRS command for Pre-amble, Burst Length and Write CRC setting. The DDR4RCD02 adjusts QxODT[1:0] dynamically if dynamic burst length on the fly function is selected in DRAM. The DDR4RCD02 assumes that all ranks are configured identically for Write/Read Pre-amble, Burst Length and Write CRC and may monitor DRAM MRS commands for only rank 0.

2.7 Power saving modes

The device supports different power saving mechanisms.

When both inputs CK_t and CK_c are being held LOW the device stops operation and enters low-power static and standby operation. It stops its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0 and QBCKE1 which are kept driven LOW. Before the device is taken out of standby operation by applying a stable input clock signal, the register inputs DCS[n:0]_n must be pulled HIGH to prevent accidental access to the control registers and DCKE0 as well as DCKE1 must be pulled LOW for a certain period of time (t_{ACT}). The input clock must be stable for a time (t_{STAB}) before any access to the device takes place. Stopping the clocks (CK_t=CK_c=LOW) will only put the DDR4RCD02 in the low-power mode and will not clear the content of the Control Words. The command mode registers will reset only when DRST_n is driven LOW.

A weak drive feature can be enabled by setting the corresponding bit in the control register. This causes the device to monitor all the DCS[n:0]_n inputs and weakly drive all outputs corresponding with the chip select gated inputs when all the DCS[n:0]_n inputs are HIGH. If any one of the DCS[n:0]_n input is LOW, the Qn outputs will function normally.

Once all the DCS[n:0]_n inputs are HIGH, the gated address command inputs to the register can float to conserve input termination power. DCKE0, DCKE1, DODT0 and DODT1 need to be driven by the system all the time.

The DRST_n input has priority over all other power saving mechanisms. When DRST_n is driven LOW, it will force the Qn outputs to float, deasserts the open-drain ALERT_n output, forces the QACKE0, QACKE1, QBCKE0 and QBCKE1 outputs LOW, disables Input Bus Termination (IBT) and forces BCK_t/BCK_c LOW and BCKE HIGH.

2.7.1 Register CKE Power Down

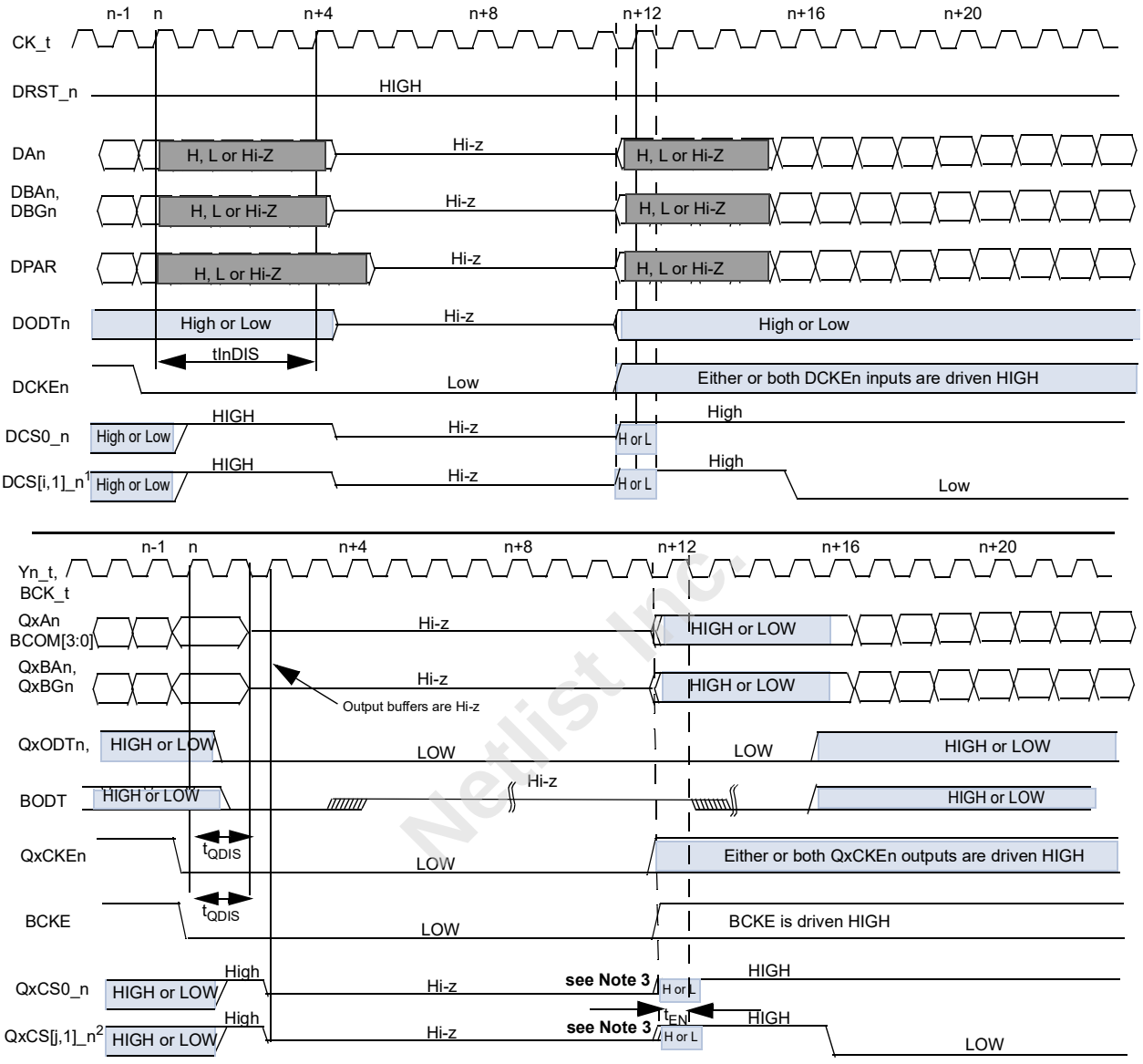
The DDR4RCD02 monitors both DCKEn input signals and enters into power saving state when it latches LOW on both DCKEn inputs and at least one of the DCKEn input has transitioned from HIGH to LOW. If either input Chip Select signal, DCS[n:0]_n, is asserted together with DCKEn, the DDR4RCD02 transfers the corresponding command to its outputs together with QxCKEn LOW, after the command latency adder programmed into F0RC0F.

There are two modes of CKE Power Down selected by control word F0RC09. Bit DA2 in F0RC09 indicates whether register turns off IBT or keeps IBT on.

The statements about DODTn and QxODTn in the remainder of this section assume that the DODTn inputs and QxODTn outputs are enabled in F0RC8x. If a DODTn input is disabled in F0RC8x, it is always disabled, even in CKE power down mode. If a QxODTn output is disabled in F0RC8x, it is always disabled, even in CKE power down mode.

2.7.1.1 Register CKE Power Down with IBT Off

Upon entry into CKE Power Down mode with IBT off, all register input buffers are disabled except for CK_t/CK_c, DCKEn and DRST_n. Upon entry into CKE Power Down mode with IBT off, IBT will be off on all inputs except DCKEn. The DDR4RCD02 disables input buffers within t_{InDIS} clocks after latching both DCKEn LOW. In order to eliminate any false parity check error, the DPAR input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS}, the register can tolerate floating input except for CK_t/CK_c, DCKEn and DRST_n. The DDR4RCD02 also disables all its output buffers except for Yn_t/Yn_c, QxODTn, QxCKEn and BCKE. The Yn_t/Yn_c outputs continue to drive a valid phase accurate clock signal. The QxODTn, QxCKEn and BCKE outputs are driven LOW. The register output buffers are HI-Z t_{QDIS} clock after QxCKEn is driven LOW. This is shown in Figure 13. Note that t_{QDIS} only starts when both QxCKEn outputs are driven low, i.e. it is delayed by the Command Latency Adder (CLA) in F0RC0F.



(1) i only applies in direct QuadCS mode. When the device is configured in this mode, i = 3.
(2) j only applies in direct QuadCS or encoded QuadCS modes. When the device is configured in these modes, j = 3.
(3) Upon CKE Power Down exit, QxCSy_n may follow DCSx_n inputs for maximum of CLA (Command Latency Adder from F0RC0F) and be held HIGH for the remainder of $t_{Fixedoutput}$ regardless of what DCSx_n input level is. For all other operation QxCSy_n outputs will follow DCSx_n inputs.

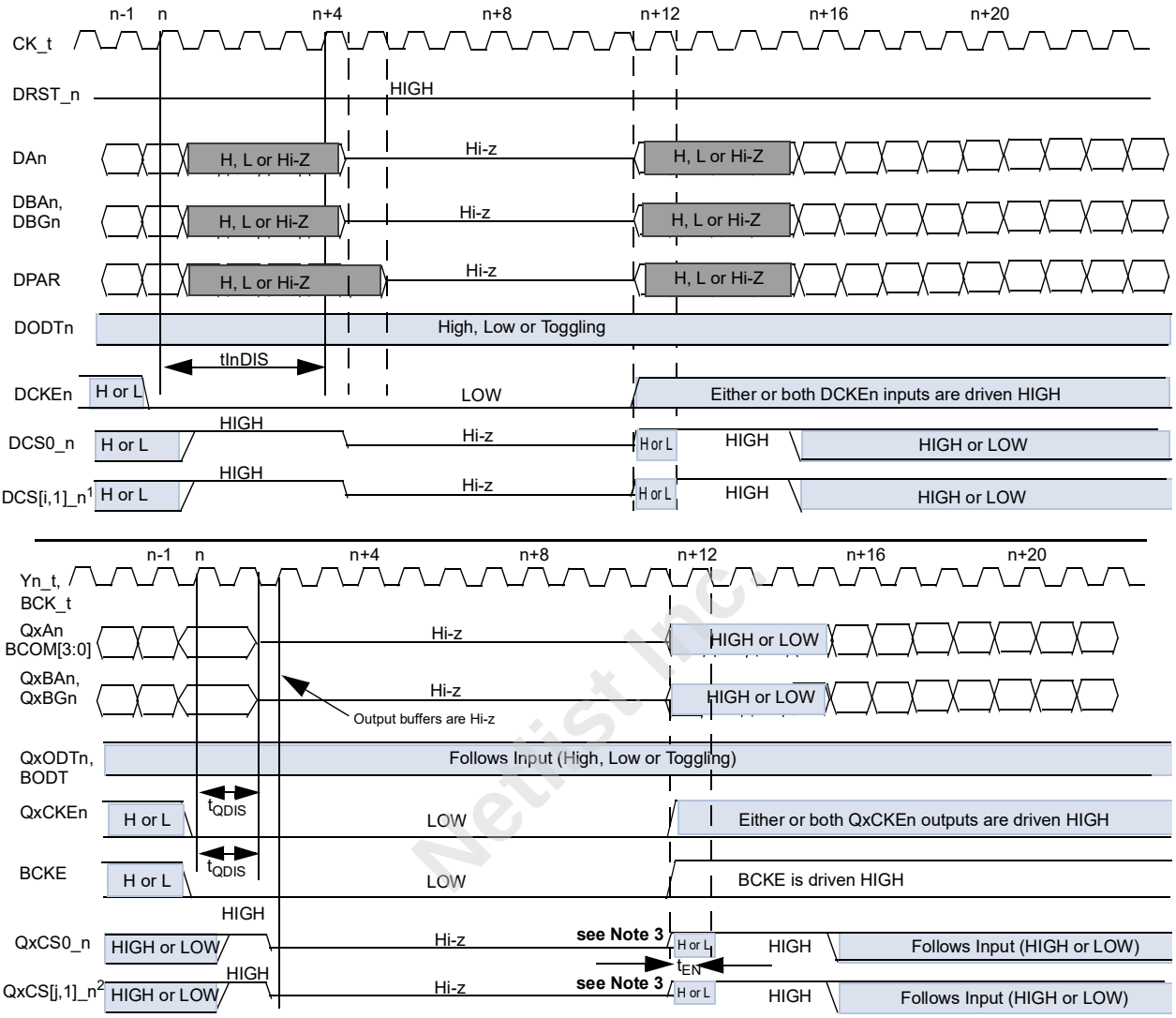
Figure 13 — Power Down Mode Entry and Exit with IBT Off

To re-enable the register from this power saving state, valid logic levels are required at all register inputs when either or both DCKEn input are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the register immediately (i.e. without the command latency adder in F0RC0F) starts driving HIGH on the appropriate QxCKEn signals and the BCKE output. The QxCSy_n signals are driven HIGH and QxODTn signals are driven LOW. Other output signals QxA[17:0], QxBA[1:0], QxBG[1:0], QxACT_n, QxC2 and QxPAR are driven either HIGH or LOW to ensure stable

valid logic on all register outputs when QxCKEn goes HIGH. The data buffer communications and control signals BCOM[3:0] are also driven either HIGH or LOW, i.e. at a valid logic level unless F0RC0D DA2 = 1. The register drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register outputs follow their corresponding input levels. BODT is driven LOW during $t_{Fixedoutput}$ and driven afterwards at the logical OR level of the DODT0 and DODT1 inputs unless F0RC8x DA7 = 1 or DA5 = 1. When exiting CKE power down mode, either one of the Chip select register inputs DCSn_n can be asserted for CLA*tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn_n can be asserted for CLA*tCK. The register guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 13.

2.7.1.2 Register CKE Power Down with IBT On

Upon entry into CKE Power Down mode with IBT on, all register input buffers are disabled except for CK_t/CK_c, DCKEn, DODTn, ERROR_IN_n and DRST_n. Upon entry into CKE Power Down mode with IBT on, IBT will remain on for all inputs. The DDR4RCD02 disables input buffers within t_{InDIS} clocks after latching both DCKEn LOW. In order to eliminate any false parity check error, the DPAR input buffer has to be kept active for 1 tCK after the Address and Command input buffers are disabled. After t_{InDIS}, the register can tolerate floating input except for CK_t/CK_c, DCKEn, DODTn and DRST_n. The DDR4RCD02 also disables all its output buffers except for Yn_t/Yn_c, QxODTn, QxCKEn, BODT and BCKE. The Yn_t/Yn_c outputs continue to drive a valid phase accurate clock signal. The QxCKEn and BCKE outputs are driven LOW. The register output buffers are hi-z t_{QDIS} clock after QxCKEn is driven LOW. This is shown in Figure 14. Note that t_{QDIS} only starts when both QxCKEn outputs are driven low, i.e. it is delayed by the Command Latency Adder (CLA) in F0RC0F.



(1) i only applies in direct QuadCS mode. When the device is configured in this mode, i = 3.
(2) j only applies in direct QuadCS or encoded QuadCS modes. When the device is configured in these modes, j = 3.
(3) Upon CKE Power Down exit, QxCSy_n may follow DCSx_n inputs for maximum of CLA (Command Latency Adder from F0RC0F) and be held HIGH for the remainder of $t_{Fixedoutput}$ regardless of what DCSx_n input level is. For all other operation QxCSy_n outputs will follow DCSx_n inputs.

Figure 14 — Power Down Mode Entry and Exit with IBT On

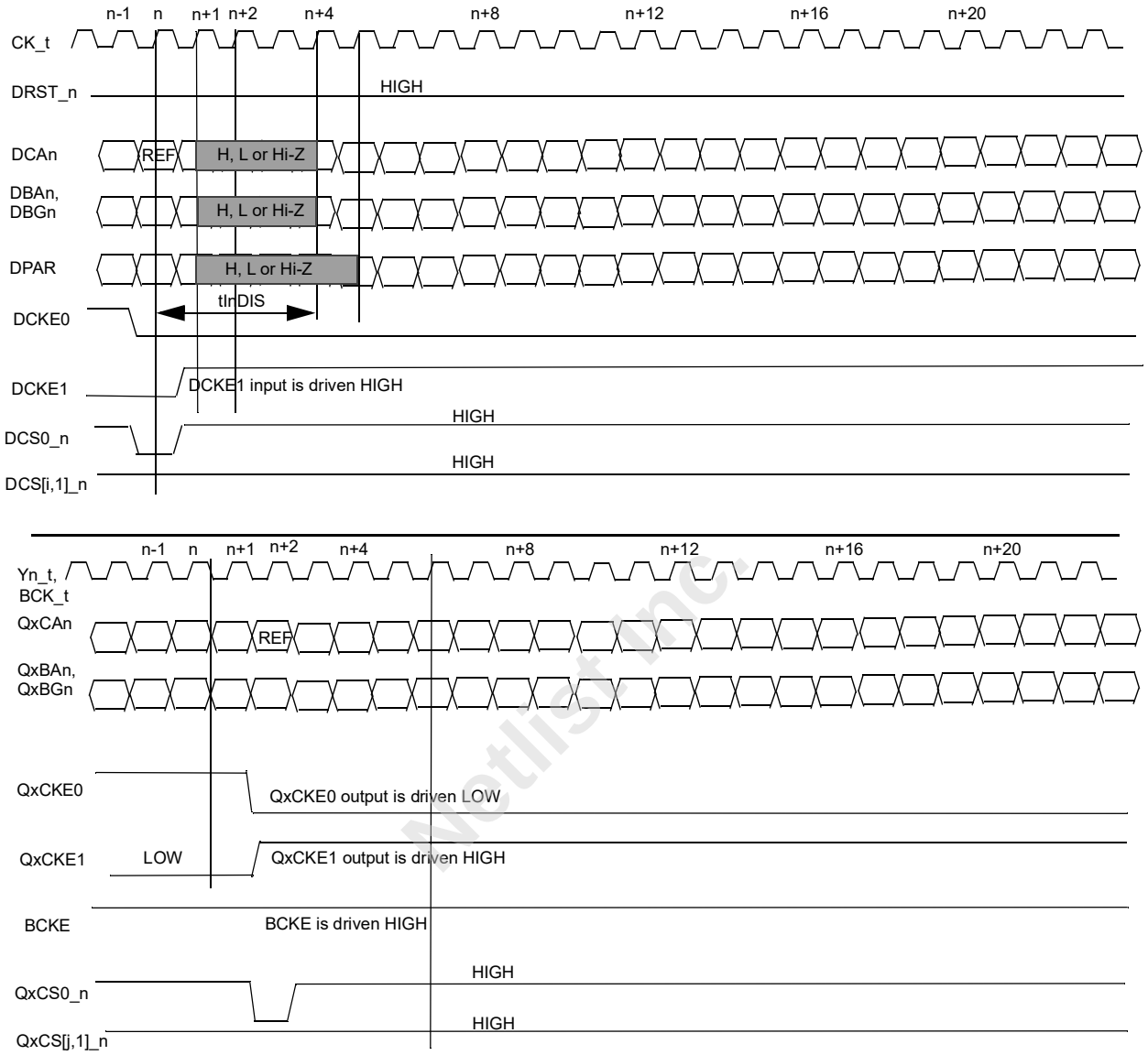
To re-enable the DDR4RCD02 from this Power Down Mode with IBT on, valid logic levels are required at all device inputs when either or both DCKEn inputs are driven HIGH. Upon either DCKE0 or DCKE1 input going HIGH, the DDR4RCD02 immediately (i.e. without the command latency adder in F0RC0F) starts driving HIGH on the appropriate QxCKEn signals and the BCKE output. The QxCSn_n signals are driven HIGH and the QxODTn signals follow the inputs. Other output signals QxA[17:0], QxBA[1:0], QxBG[1:0], QxACT_n, QxC2 and QxPAR are driven either HIGH or LOW to ensure stable valid logic on all device outputs when QxCKEn goes HIGH. The data buffer communications and control signals BCOM[3:0] are also driven either HIGH or LOW, i.e. at a valid logic level unless F0RC0D DA2 = 1. The register drives output signals to these levels for $t_{Fixedoutput}$ to allow input receivers to be stabilized. After the input receivers are stabilized, the register outputs follow their corresponding input levels.

BODT is driven at the logical OR level of the DODT0 and DODT1 inputs unless F0RC8x DA7 = 1 or DA5 = 1. When exiting CKE power down mode, either one of the Chip select register inputs DCSn_n can be asserted for CLA*tCK. For QuadCS capable register, when working in quad rank mode, either two of the Chip select register inputs DCSn_n can be asserted for CLA*tCK. The device guarantees that input receivers are stabilized within $t_{Fixedoutput}$ clocks after DCKEn input is driven HIGH. This is shown in Figure 14.

The previous diagrams showed CKE power down entry and exit with a Command Latency Adder (CLA) of 0. With a non-zero CLA the CKE power down mode entry is delayed by CLA*tCK w.r.t. the RCD outputs, i.e. the outputs are tristated later. The delay caused by CLA also applies to the DRAM Power Down Entry (PDE) and Self Refresh Entry (SRE) since both commands as well as the falling CKE edge are delayed on the RCD outputs. Input disable is just based on the DCKEn timing, i.e. the inputs are disabled at the same time as without a command latency adder. Power down mode exit is also based on the DCKEn inputs, i.e. the RCD CKE power down mode exit (as well as the DRAM Power Down Exit and Self Refresh Exit) is not delayed by CLA. Therefore special consideration needs to be given to the case when the duration of the RCD CKE power down mode is less than the Command Latency Adder CLA, i.e. when the LOW overlap between DCKE0 and DCKE1 is less or equal than CLA. This case is shown in Figure 15 which depicts single cycle LOW overlap between DCKE0 and DCKE1 with a Command Latency Adder of 1.

Since forwarding the rising edge of CKE is not delayed by CLA, there is no LOW overlap between QxCKE0 and QxCKE1 and hence the output side of the RCD never enters power down mode. However, the inputs of the RCD start to disable when registering both DCKE inputs LOW in the same cycle. During $t_{Fixedoutput}$ (which is triggered by the rising edge of one of the DCKE inputs), the RCD is required to follow all inputs for the duration of CLA. This ensures that any commands the RCD captures while both DCKE inputs are sampled LOW are forwarded to the outputs.

The duration of $t_{Fixedoutput}$ depends on CLA which ensures that the RCD holds the QxCSy_n outputs HIGH during the last few cycles of $t_{Fixedoutput}$ which correspond to the time when the RCD inputs may have been disabled.



(1) i only applies in direct QuadCS mode. When the device is configured in this mode, i = 3.
(2) j only applies in direct QuadCS or encoded QuadCS modes. When the device is configured in these modes, j = 3.
(3) Upon CKE Power Down exit, QxCSy_n must follow DCSx_n inputs for maximum of CLA (Command Latency Adder from F0RC0F) and then be held HIGH for the remainder of $t_{Fixedoutput}$ regardless of what DCSx_n input level is. For all other operation QxCSy_n outputs will follow DCSx_n inputs.

Figure 15 — Single Cycle Power Down Mode Entry and Exit with CLA=1

2.7.2 Clock Stopped Power Down Mode

To support S3 Power Management mode or any other operation that allows Yn_t clocks to float, the DDR4RCD02 supports a Clock Stopped power down mode. When both inputs CK_t and CK_c are being held LOW (i.e. below $V_{IL\ (static)}$) or float (when they will eventually settle at LOW because of the 10 kΩ to 100 kΩ pull-down resistor in the CK_t/CK_c input buffer), the device stops operation and enters low-power static and standby operation. The corresponding timing requirement are shown in Figure 16, "Clock Stopped Power Down Entry and Exit with IBT On" and Figure 17, "Clock Stopped Power Down Entry and Exit with IBT Off". The register device will stop its PLL and floats all outputs except QACKE0, QACKE1, QBCKE0, QBCKE1, BCK_t/BCK_c and BCKE (which must be kept driven LOW) unless the buffer control bus is disabled in F0RC0D. The device deasserts the open-drain ALERT_n output in clock stopped power down mode. The Clock Stopped power down mode can only be utilized once the DRAM received a self refresh command. In this state, the DRAM ignores all inputs except CKE. Hence, all register outputs besides QxCKE0,QxCKE1, BCK_t/BCK_c and BCKE can be disabled.

2.7.2.1 Clock Stopped Power Down Mode Entry

To enter Clock Stopped Power Down mode, DCKEn will be deasserted for a minimum of one tCKoff before pulling CK_t and CK_c LOW. After holding CK_t and CK_c LOW (i.e. below $V_{IL\ (static)}$) for at least one tCKEV, both CK_t and CK_c can be floated. Because of the 10 kΩ to 100 kΩ pull-down resistor in the CK_t/CK_c input buffer, CK_t/CK_c will stay at LOW even though they are not being driven. The register is now in Clock Stopped Power Down mode. If the buffer control bus is enabled in F0RC0D, the RCD drives BCK_t/BCK_c and BCKE LOW while in Clock Stopped Power Down mode. After CK_t and CK_c are pulled LOW, DCKEn will remain LOW for at least one tCKEV before it can be floated. At this point, all input receivers and input termination of the DDR4RCD02 are disabled. The only active input circuits are CK_t and CK_c, which are required to detect the wake up request from the host.

2.7.2.2 Clock Stopped Power Down Mode Exit

To wake up the register after entering Clock Stopped Power Down, the register inputs DCS0_n must be driven to HIGH (to prevent accidental access to the control registers), and DCKEn to LOW. After that, a frequency and phase accurate input clock signal must be applied. The state of the DCS[n:0]_n inputs must not be changed before the end of tSTAB. The input clock CK_t/CK_c must be stable for a time equal or greater than tSTAB before any access to the DDR4RCD02 can take place.

If the buffer control bus is enabled in F0RC0D, the RCD drives BCKE, BCK_t and BCK_c LOW during tSTAB.

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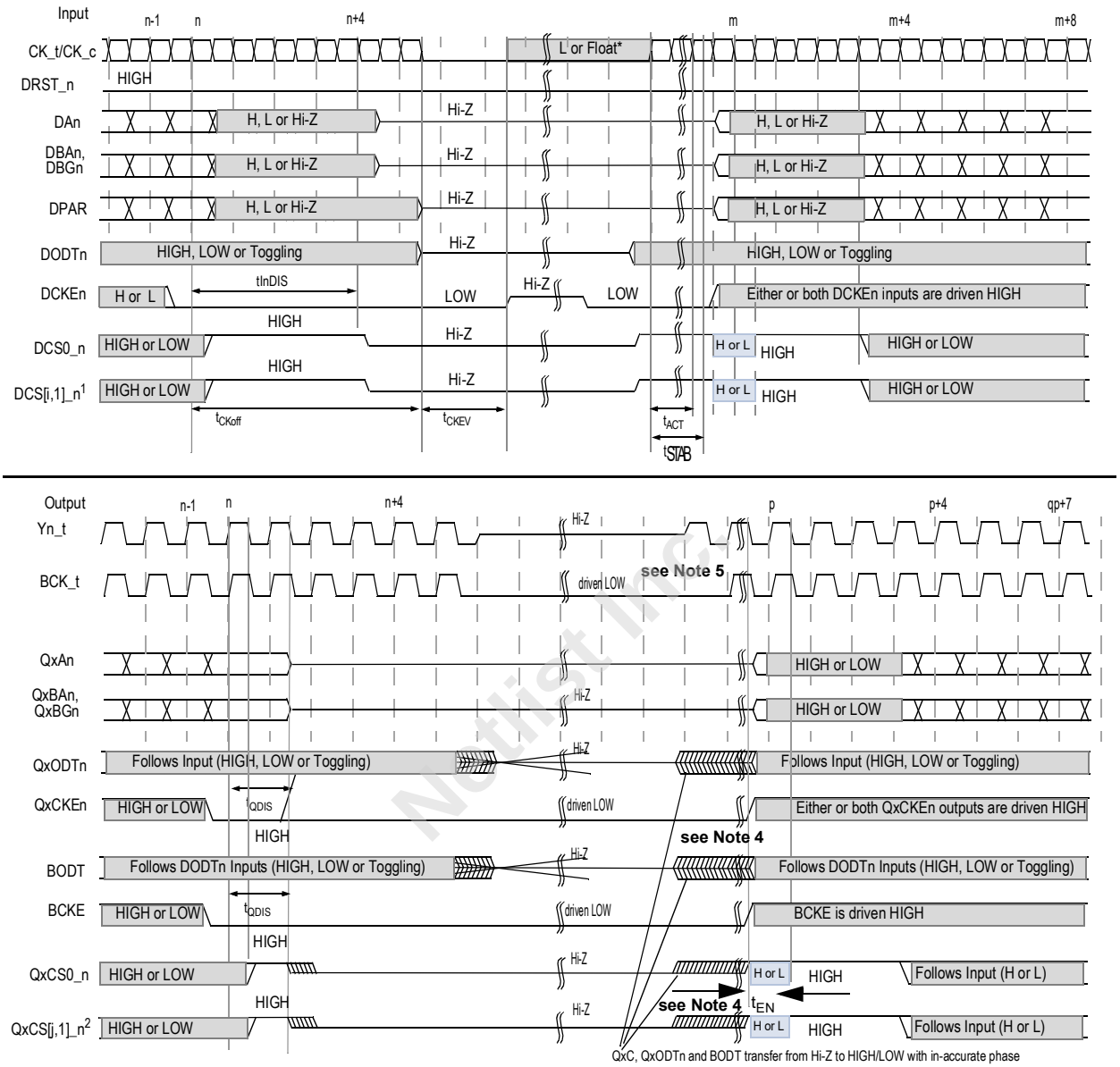
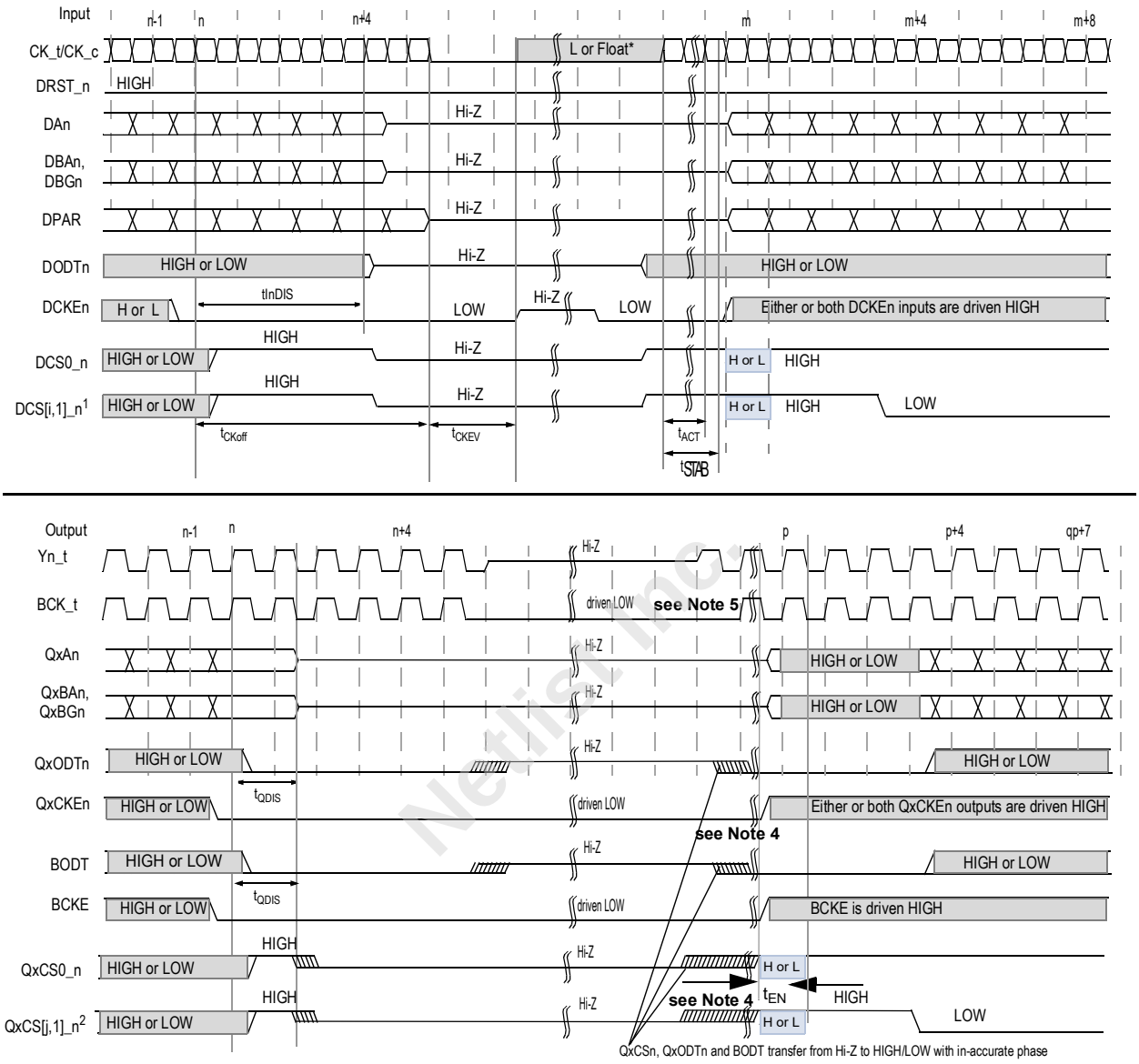


(1) i only applies in direct QuadCS mode. When the device is configured in this mode, i = 3.
(2) j only applies in direct QuadCS or encoded QuadCS modes. When the device is configured in these modes, j = 3.
(3) When CK_t/CK_c inputs are floated, CK_t/CK_c inputs are pulled LOW by the (10 kΩ to 100 kΩ) pull-down resistor in the CK_t/CK_c input buffer.
(4) Upon CKE Power Down exit, QxCSy_n may follow DCSx_n inputs for maximum of 1 tCK, or be held HIGH for $t_{Fixedoutput}$ regardless of what DCSx_n input level is. For all other operation QxCSy_n outputs will follow DCSx_n inputs.
(5) BCK_t/BCK_c shall be stable before the end of t_{STAB}.

Figure 16 — Clock Stopped Power Down Entry and Exit with IBT On



(1) i only applies in direct QuadCS mode. When the device is configured in this mode, i = 3.
(2) j only applies in direct QuadCS or encoded QuadCS modes. When the device is configured in these modes, j = 3.
(3) When CK_t/CK_c inputs are floated, CK_t/CK_c inputs are pulled LOW by the (10 kΩ to 100 kΩ) pull-down resistor in the CK_t/CK_c input buffer.
(4) Upon CKE Power Down exit, QxCSy_n may follow DCSx_n inputs for maximum of 1 tCK, or be held HIGH for $t_{Fixedoutput}$ regardless of what DCSx_n input level is. For all other operation QxCSy_n outputs will follow DCSx_n inputs.
(5) BCK_t/BCK_c shall be stable before the end of t_{STAB}.

Figure 17 — Clock Stopped Power Down Entry and Exit with IBT Off

2.8 Dual Frequency Support

The DDR4 register supports operation at a second, i.e. lower than nominal, frequency as a means to save buffer and DRAM power when the memory bandwidth demand allows.

To enable fast frequency switching without the need for retraining every time the frequency is changed, the DDR4 register can be trained twice at two different frequencies at boot up time and retain register settings associated with each of the two frequencies. These two sets of registers consist of F0RC03, F0RC04, F0RC05, F0RC0F, F0RC1x, F0RC5x DA[3:0], F0RC7x, F0RC8xDA[4:0], F0RC9x, F0RCAx, F1RC00, F1RC1x, F1RC2x, F1RC3x, F1RC4x, F1RC5x, F1RC6x, F1RC7x, F1RC8x, and F1RC9x. The RCD hardware will take care of updating any other frequency-dependent internal settings in each frequency context as needed.

Switching between the two frequency contexts is achieved by writing to control word F0RC0A bit DA3. DA3='0' selects the default frequency context 1 while DA3='1' selects frequency context 2.

Dual frequency training at boot up time requires selecting the appropriate frequency context, performing the training at that frequency and then selecting the other frequency context and performing the training at the other frequency. Subsequently, every time the operation frequency changes, the corresponding frequency context bit must be set in the DDR4 register via control word writes to F0RC0A and F0RC3x. The control word writes to F0RC0A/F0RC3x must be the last access to the DDR4 register before the input frequency on the CK_t/CK_c pins changes. In addition the DRAMs must be put in self refresh mode and the DDR4RCD02 must be put into clock stopped power down mode before the frequency change occurs and the entire frequency change procedure specified in the DDR4 DRAM specification must be followed.

2.8.1 Input Clock Frequency Change

Once the DDR4RCD02 is initialized, the DDR4RCD02 requires the clock to be stable during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the stable state, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate only by going through Clock stop power down mode. DDR4RCD02 allows two possible sequences (Sequence A and Sequence B) for input clock frequency change. The exact sequence of steps for an input frequency change to an RDIMM is outlined below. Note that additional steps are required for an input frequency change to an LRDIMM and they are documented in the DDR4DB02 specification.

Sequence A:

1. Disable CKE power down mode in the RCD (i.e. write to F0RC09, bit 3 = 0)
2. Put the DRAMs into Self Refresh by sending SRE commands to all ranks. After this step all DCKE inputs will be LOW but the RCD will stay active.[1]
3. Send new F0RC0A and F0RC3x frequency setting to RCD without asserting CKE. The control word writes will proceed because RCD is still active. DRAMs are still in Self Refresh. No additional commands to the RCD are allowed after this step (until step 6).
4. Host changes frequency by going through Clock Stopped mode. Both CK inputs need to be driven LOW (i.e. below $V_{IL(static)}$) for a minimum of t_{CKEV} before the clock frequency may change. The DDR4RCD02 input clock frequency is allowed to change only within range between the minimum and maximum application or test frequencies specified in Table 141.

1. Since the CMD/ADD input receivers of the RCD will remain enabled after the DCKEn input signals go LOW, the host is responsible for driving valid signals and Deselect command (DCSy_n all HIGH) before and after the Clock Stopped Power Down entry and exit events.

5. The DCKE inputs must be held at stable LOW levels during t_{CKEV} and during the t_{STAB} time after the clock signals are restarted.
6. Assert CKE and exit DRAM Self Refresh.
7. Depending on the new clock frequency, additional MRS commands to the DRAM may need to be issued to appropriately set CL, AL, and CWL with BCKE continuously registered high. RCD CKE power down mode may be re-enabled.

Sequence B:

1. Send new F0RC0A and F0RC3x frequency setting to RCD. The RCD ensures application of the new setting at or prior to next rising edge of DCKE.
2. Put the DRAM into Self Refresh by sending SRE commands to all ranks. After this step all DCKE inputs will be LOW.
3. Host changes frequency by going through Clock Stopped mode. Both CK inputs need to be driven LOW (i.e. below VIL(static) for a minimum of tCKEV before the clock frequency may change. The DDR4 RCD02 input clock frequency is allowed to change only within range between the minimum and maximum application or test frequencies specified in Table 141.
4. The DCKE inputs must be held at stable LOW levels during tCKEV and during tSTAB time after the clock signals are restarted.
5. Assert CKE and exit DRAM Self Refresh.
6. Depending on the new clock frequency, additional MRS commands to the DRAM may need to be issued to appropriately set CL, AL, and CWL with BCKE continuously registered high.

2.9 Output Inversion Enabling/Disabling

Output Inversion is enabled by default, after DRST_n is de-asserted, to conserve power and reduce simultaneous output switching current. All A-outputs will follow the equivalent inputs. The DDR4 register output signals are divided into two classes: signals that can be inverted (e.g. regular addresses) and signals that cannot be inverted (because they have a special function) - see Figure 18. Only the following 14 signals in the first class will be driven to the complement of the matching A-outputs: QBA3 to QBA9, QBA11, QBA13, QBA17, QBBA0 to QBBA1 and QBBG0 to QBBG1.

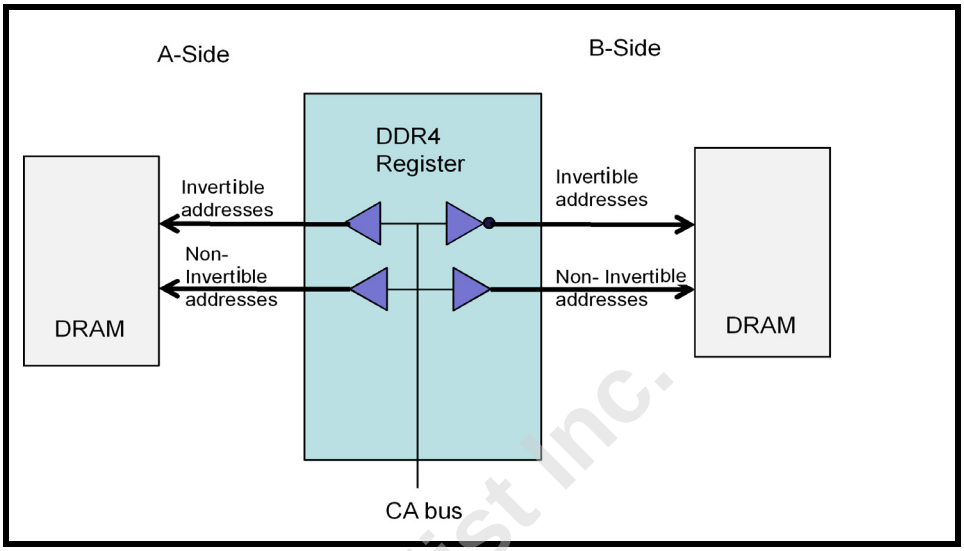


Figure 18 — Output Inversion Functional Diagram

The Output Inversion feature is always enabled, even during DRAM MRS commands. In order to ensure that the DRAM receives the correct (i.e. uninverted) MRS bits, the host-to-register-to-DRAM MRS programming is split into a two-step process - see Figure 19. In the first step the A-side DRAMs are programmed using non-inverted addresses from the host. In the second step the B-side DRAMs are programmed using inverted addresses for the invertible address signals and non-inverted addresses for the non-invertible address signals from the host.

When the DDR4 register decodes the MRS command (DACT_n = 1, DA16/RAS_n = 0, DA15/CAS_n = 0, DA14/WE_n = 0 and only one DCSx_n = 0), it will use the state of the DBG1 input to gate the assertion of the output chip selects QxCSy_n. When DBG1 = 0 it will enable the QACSy_n outputs to select the A-side DRAMs and when DBG1 = 1 it will enable the QBCSy_n outputs to select the B-side DRAMs. The DDR4RCD02 will drive the QACA and QBCA outputs (minus the disabled chip selects) regardless of which input level is sampled on DBG1.

When a DIMM utilizes address mirroring (as indicated in the SPD bytes for the module), DBG0 will be used by the register instead of DBG1 as an A-side/B-side indication for MRS command to odd ranks.

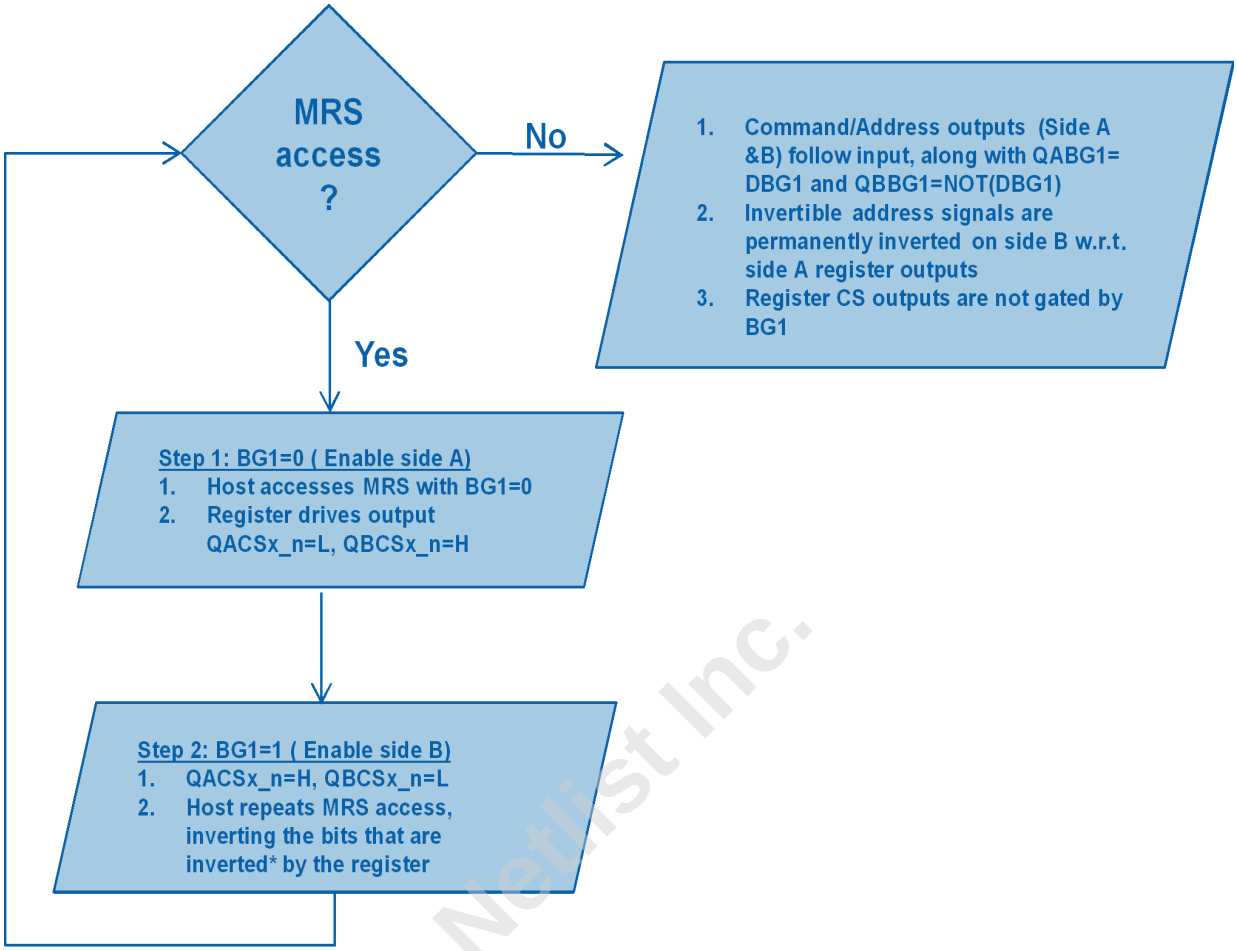


Figure 19 — Address Inversion Flow-chart

The following is the address map for address inversion.

Table 13 — Address Inversion

Host bit (RCD input)	A-side DRAM connection	B-side DRAM connection	
DA0	A0	A0	A0 not inverted as it affects the burst start
DA1	A1	A1	A1 not inverted as it affects the burst start
DA2	A2	A2	A2 not inverted as it affects the burst start
DA3	A3	NOT (A3)	Inverted
DA4	A4	NOT (A4)	
DA5	A5	NOT (A5)	
DA6	A6	NOT (A6)	
DA7	A7	NOT (A7)	
DA8	A8	NOT (A8)	
DA9	A9	NOT (A9)	
DA10	A10	A10	A10 cannot be inverted as it is Auto Precharge
DA11	A11	NOT (A11)	Inverted
DA12	A12	A12	A12 cannot be inverted as it is Burst Length
DA13	A13	NOT (A13)	Inverted
DA14	A14	A14	A14 cannot be inverted as it is WE_n
DA15	A15	A15	A15 cannot be inverted as it is CAS_n
DA16	A16	A16	A16 cannot be inverted as it is RAS_n
DA17	A17	NOT (A17)	Inverted
DBA0	BA0	NOT (BA0)	
DBA1	BA1	NOT (BA1)	
DBG0	BG0	NOT (BG0)	
DBG1	BG1	NOT (BG1)	

The DDR4RCD02 does not support on-the-fly Fine Granularity Refresh (OTF FGR) for DDR4 DRAMs on DIMMs that utilize the B-side outputs since the OTF FGR modes are encoded using the logic level on BG0 and the QBBG0 output is inverted relative to the DBG0 input.

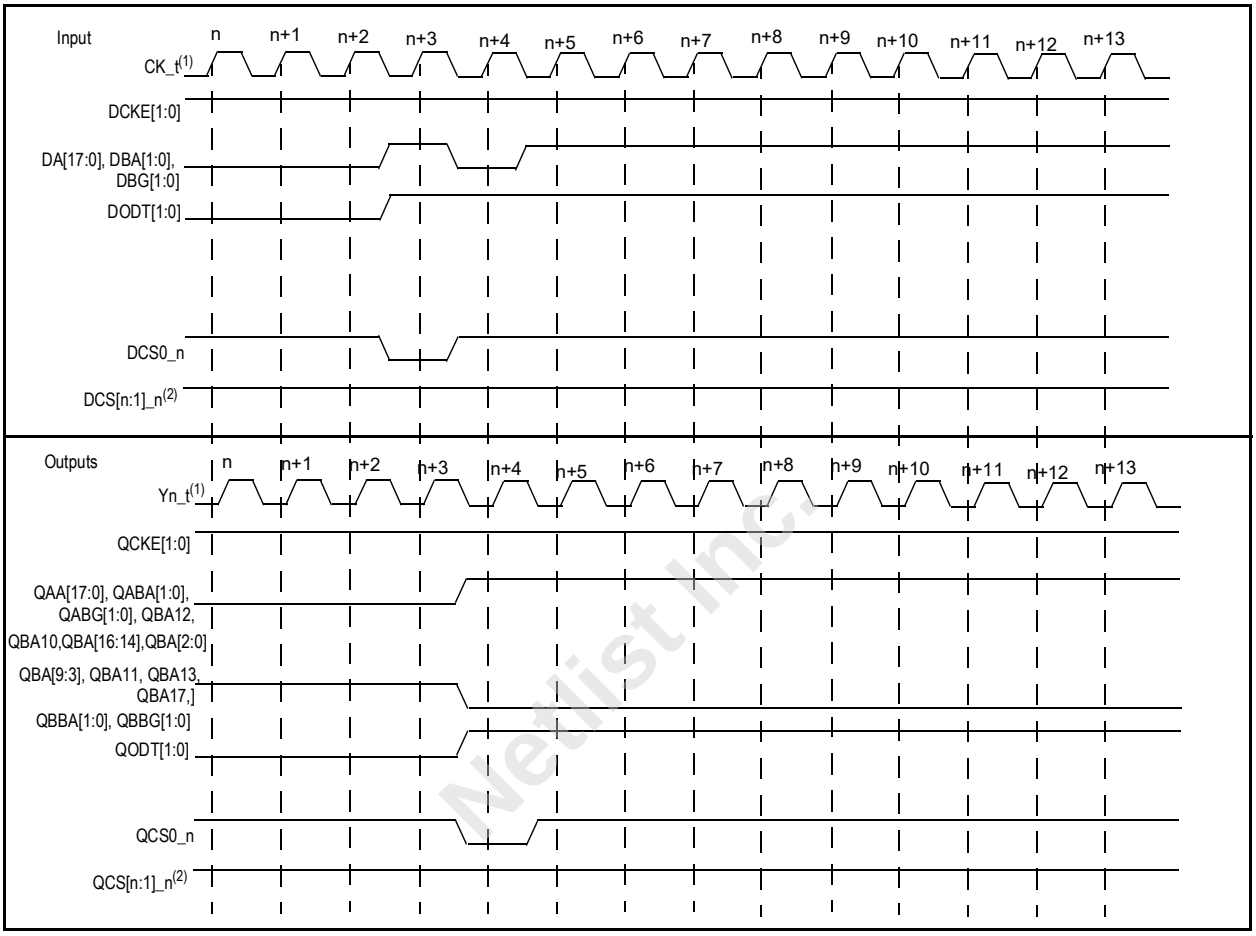
The following is the address map for address mirroring and address inversion.

Table 14 — Address Mirroring and Inversion

Host bit (RCD input)	Register output	A-side Even rank DRAM connection	B-side Even rank DRAM connection	A-side Odd rank DRAM connection, Mirroring off.	A-side Odd Rank DRAM connection, Mirroring on	B-side Odd rank DRAM connection, Mirroring off.	B-side Odd Rank DRAM connection, Mirroring on
DA0	QxA0	A0	A0	A0	A0	A0	A0
DA1	QxA1	A1	A1	A1	A1	A1	A1
DA2	QxA2	A2	A2	A2	A2	A2	A2
DA3	QxA3	A3	NOT (A3)	A3	**A4**	NOT (A3)	**NOT (A4)**
DA4	QxA4	A4	NOT (A4)	A4	**A3**	NOT (A4)	**NOT (A3)**
DA5	QxA5	A5	NOT (A5)	A5	**A6**	NOT (A5)	**NOT (A6)**
DA6	QxA6	A6	NOT (A6)	A6	**A5**	NOT (A6)	**NOT (A5)**
DA7	QxA7	A7	NOT (A7)	A7	**A8**	NOT (A7)	**NOT (A8)**
DA8	QxA8	A8	NOT (A8)	A8	**A7**	NOT (A8)	**NOT (A7)**
DA9	QxA9	A9	NOT (A9)	A9	A9	NOT (A9)	NOT (A9)
DA10	QxA10	A10	A10	A10	A10	A10	A10
DA11	QxA11	A11	NOT (A11)	A11	**A13**	NOT (A11)	**NOT (A13)**
DA12	QxA12	A12	A12	A12	A12	A12	A12
DA13	QxA13	A13	NOT (A13)	A13	**A11**	NOT (A13)	**NOT (A11)**
DA14	QxA14	A14	A14	A14	A14	A14	A14
DA15	QxA15	A15	A15	A15	A15	A15	A15
DA16	QxA16	A16	A16	A16	A16	A16	A16
DA17	QxA17	A17	NOT (A17)	A17	A17	NOT (A17)	NOT (A17)
DBA0	QxBA0	BA0	NOT (BA0)	BA0	**BA1**	NOT (BA0)	**NOT (BA1)**
DBA1	QxBA1	BA1	NOT (BA1)	BA1	**BA0**	NOT (BA1)	**NOT (BA0)**
DBG0	QxBG0	BG0	NOT (BG0)	BG0	**BG1**	NOT (BG0)	**NOT (BG1)**
DBG1	QxBG1	BG1	NOT (BG1)	BG1	**BG0**	NOT (BG1)	**NOT (BG0)**

2.9.1 1T Timing Only

Unlike the SSTE32882 DDR3 register that supported 3T timing for MRS commands, the DDR4RCD02 only supports 1T timing. The inputs and outputs relationships are shown Figure 20.



(1) CK_c and Yn_c left out for better visibility
(2) n=1 for QuadCS disabled, n=3 for QuadCS enabled

Figure 20 — Timing During Normal Operation

2.10 ZQ Calibration

ZQ Calibration command is used to calibrate DDR4RCD02 Ron and IBT values. DDR4RCD02 needs longer time to calibrate output driver and input bus termination values at initialization and relatively smaller time to perform periodic calibration. In order to use ZQ calibration command, a 240 Ω +/- 1 % resistor must be connected between the ZQCAL pin and Vss.

The DDR4RCD02 snoops the CA bus for ZQCL and ZQCS commands to DRAMs and may use the tZQinit (for the first ZQCL command after reset), tZQOper (for all subsequent ZQCL commands) and tZQCS times to perform its own Ron and IBT calibration in parallel to the DRAM's Ron and ODT calibration. If the LRDIMM disable bit in F0RC0D is reset, the RCD also forwards ZQCL or ZQCS commands to the data buffer via BCW Write commands to BC06 if it performs its own calibration. Note that the RCD may not assume that any particular rank gets regular

ZQCal commands during normal operation since any given rank (or any arbitrary subset of ranks) may be in Self-Refresh state and not require ZQCal commands.

For LRDIMM operations, the host is responsible for keeping the buffer control word F[7:0]BC7x in the DDR4DB02 cleared to '000' before ZQCL or ZQCS commands are sent to the DDR4RCD02. Otherwise writes to the DDR4DB02 Command Space control word (BC06) which is located in function space 0 (e.g. ZQCL or ZQCS commands snooped and forwarded as BCOM write commands by the DDR4RCD02) will not find their intended target.

No other activities are allowed on a DDR4 channel by the memory controller for the duration of tZQInit, tZQOper and tZQCS. Once calibration is achieved the DDR4RCD02 must disable the ZQ current path to reduce power consumption.

2.11 Latency Equalization Support

3D Stacked SDRAMs have a higher CAS latency than monolithic devices. For greater platform flexibility it is highly desirable to mix DIMMs with both 3DS and mono SDRAMs on the same DDR4 channel. Since memory controllers typically can only handle devices with equal CAS latencies in the same channel, it is required that the DDR4 register has a mechanism to increase the CAS latency of mono SDRAMs to match the CAS latency of 3DS SDRAMs. However, this mechanism only equalizes the DRAM latencies, not the total DIMM latencies. Hence this DDR4 register mechanism does not by itself allow mixing DDR4 RDIMMs and DDR4 LRDIMMs in the same channel.

To equalize different SDRAM latencies, the DDR4 register supports a programmable latency adder of 0 nCK, 1nCK, 2nCK, 3nCK or 4nCK for all DRAM commands - see conceptual diagram in Figure 2.14. The power-up default is 1nCK latency adder.

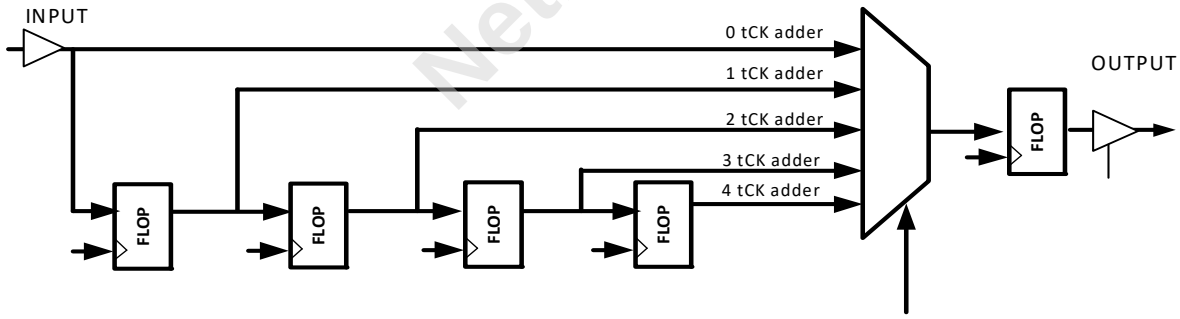


Figure 21 — Latency Equalizer Delays.

With a latency adder enabled, the DDR4 register will delay assertion of the QxCSn_n, QxCKEn, QxODTn, QxAn, QxBAn, QxBGn, QxACT_n, QxC2 and QxPAR outputs by the corresponding number of clock cycles.

2.12 Output Delay Control

The DDR4RCD02 supports output delay control for output signal groups QxCSn_n, QxCn, QxCKE, QxODT, QxCA, Y1/Y3, Y0/Y2, BCOM[3:0]/BKCE/BODT, and BCK located in F1RC1x through F1RC9x. The output delay setting are incremental CK fractions of 1/64 tCK. Each signal group can be enabled or disable independently through RCW. The Host must wait t_{ODU} after the RCW has been written to a signal group before the output becomes stable.

2.13 Output Slew Rate Control

To optimize the eye aperture at the DRAM, the DDR4RCD02 will support Slow, Moderate, and Fast output slew rates on the DRAM interface for speeds of 2933 and 3200 MT/s. The output slew rates are selected by control word writes to F1RC02, F1RC03, F1RC04 and F1RC05. Control words F1RC02 to F1RC05 must not be written for speeds of 2666 MT/s or lower.

2.14 CA Bus Training Modes

The DDR4RCD02 supports several training modes (selected in Table 44, "F0RC0C: Training Control Word") in order to assist the memory controller in aligning the incoming command/address and control signals optimally to the input clock signal CK_t/CK_t. These training modes are only available if a non-zero latency adder has been selected.

In Clock-to-CA training mode the DDR4RCD02 ORs all enabled Dn inputs[1] every other cycle together and loops back the result to the ALERT_n output pin. In this mode, the DPAR input is sampled at the same time as the other Dn inputs. The ALERT_n latency relative to the DQn inputs is the same 3 cycles as in the normal parity mode. During any of the CA bus training modes, QCA/QxCKEn and QxODTn hold their previous values and parity checking is disabled.

The memory controller can use the Clock-to-CA training mode and feedback from the DDR4RCD02 to adjust the CK_t/CK_c to Dn relationship analogous to the write leveling sequence which adjusts the DQS_t/DQS_c to CK_t/CK_c relationship. The memory controller writes consecutive sequences of all '1's and all '0's on the CA bus and pulls in the Dn timing until the DDR4RCD02 samples all Dn inputs as 0, which is indicated with the LOW assertion of ALERT_n. This position indicates the start position of a cumulative CA bus "eye opening". The memory controller advances the clock position or pulls in the Dn timing until the DDR4RCD02 samples at least one input as '1', which is indicated by ALERT_n remaining high three cycles after the last command. This position indicates the end position of a cumulative CA bus "eye opening". The memory controller can now position either the clock phase or the Dn input timing so that the clock edge is in the middle of this "eye opening" to achieve equal amounts of setup and hold time relative to the clock edge.

Figure 22 shows three sampling phase positions where the loopback ALERT_n pin transmits either a consistent 0 output, a randomly toggling 1/0 output or a consistent 1 output, indicating sampling positions at the LOW time, the transition time or the HIGH time of the inputs, respectively.

1. Includes DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DC2, DPAR, DC[1:0]

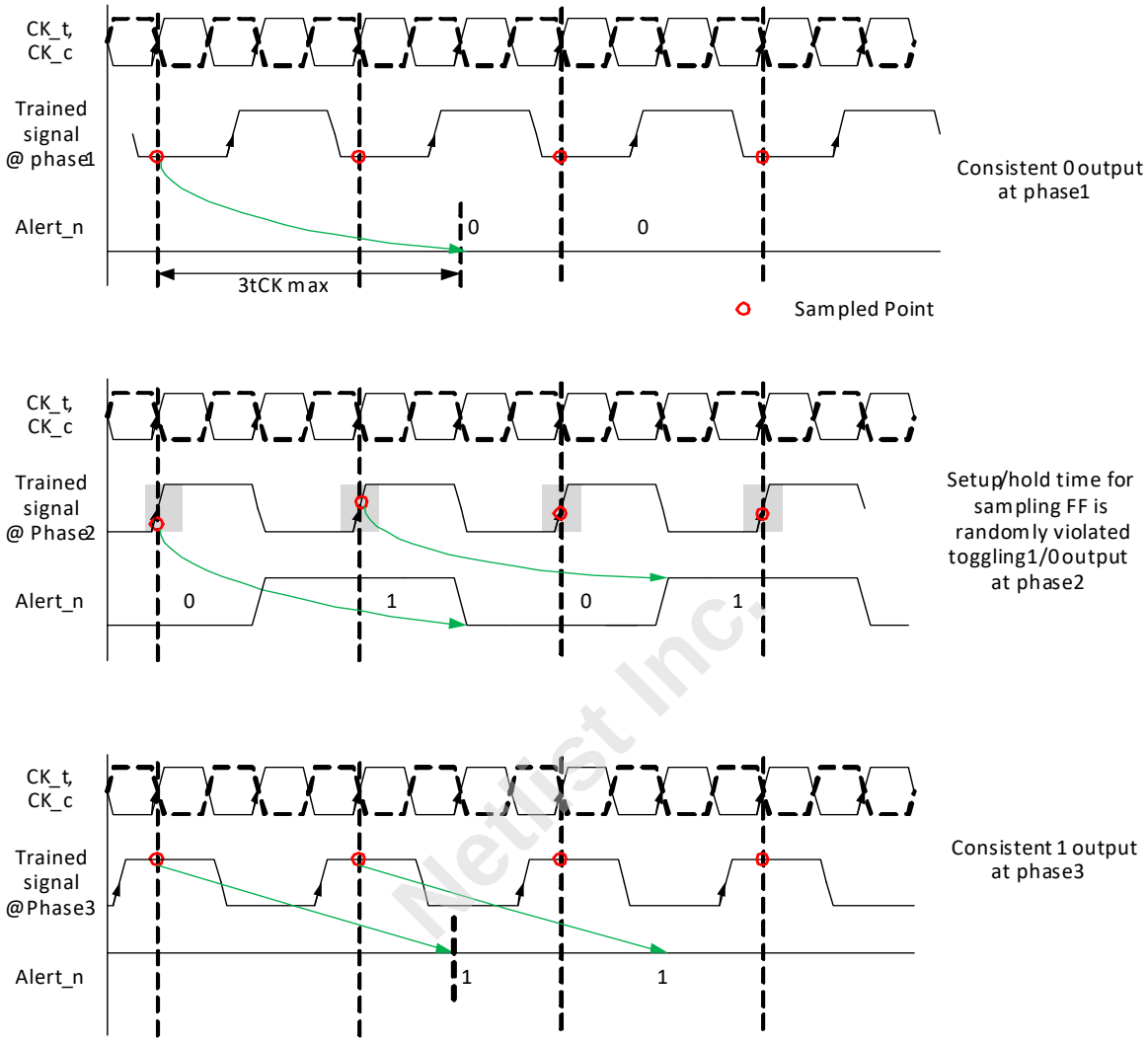


Figure 22 — Clock-to-CA Training Mode Examples

The memory controller can use the DCS0_n, DCS1_n, DCKE0, DCKE1, DODT0 and DODT0 loop back modes in similar fashion. In each of these modes a single input signal is looped back to the ALERT_n output and the memory controller can determine the optimal clock position for each of the control signals that are used for a particular DIMM. Once the optimal clock position for all CMD/ADDR and control inputs has been established, the memory controller can determine the best clock position for the whole set of input signals or potentially move the timing of individual control signals around to increase either setup or hold margins relative to the clock edge.

The DRAM is protected by driving the RCD control outputs at inactive levels. The RCD may either force all outputs than can be chip selects (including QxC0/CS2_n and QxC1/CS3_n) HIGH and all QxCKE and QxODT outputs LOW OR hold the previous values on QxCA/QxCS/QxCKE/QxODT before entering any of the CA training modes. The data buffer is protected by driving the buffer control interface signals at inactive levels. The RCD may either drive BODT and BCKE outputs LOW and BCOM[3:0] to '1010' (NOP command) OR the RCD may hold the previous values on BODT/BCKE/BCOM before entering any of the CA training modes.

The RCD does not decode commands while any F0RC0C training mode is enabled. It is thus necessary for the

register to correspondingly disable and ignore unused inputs in each training mode. The following two methods to change or exit CA training modes are supported:

(a) Write access to F0RC0C through I^2C Bus and

(b) DRST_n Reset event.

2.15 Transparent Mode

The DDR4RCD02 supports a transparent mode feature of the data buffer that enables low-speed testing of LRDIMMs.

To enter transparent mode, the host first sends a BCW write command to enable transparent mode in the DB. Then it sends a RCW write command with F0RC02, DA2 = 1 to enable transparent mode in the RCD.

While in transparent mode, the DB does not interpret BCOM commands and for BCOM[3:0] input values of '1010' it directs the data flow from host interface to DRAM interface. For BCOM[3:0] input values other than '1010' it directs the data flow from DRAM interface to host interface.

While in transparent mode, the RCD drives BCOM[3:0] statically to '1010' (NOP) when the DPAR input is LOW and to '0101' when the DPAR input is HIGH. All output signals in the RCD, other than BCOM[3:0], continue working as they do in the normal mode of operation. In other words, all the RCD features and functions not directly related to BCOM[3:0] remain operational in transparent mode. In addition, all the clock frequencies and PLL operational modes available in normal mode will also be supported in transparent mode.

To exit transparent mode, the host sends a RCW write command with F0RC02, DA2=0 to exit RCD transparent mode followed by issuing a DB reset command via RC06 to exit the DDR4DB02 transparent mode.

2.16 Control Gear-down Mode (CGM)

Control Gear-down Mode provides the ability to slow down (gear down) the control signals (CS_n, CKE, ODT) to operate in a 2N mode vs 1N. At some higher frequencies of DDR4, 1N control timings on the pre- and post-register bus may not be feasible depending on system configuration.

The DDR4RCD02 defaults to 1/2 rate (1N) clock mode at power up/reset. General sequence for initiating Control Gear-down (2N) Mode during initialization:

1. DDR4RCD02 (and DRAM) defaults to 1/2 rate (1N) mode at power up/reset.
2. Deassertion of DRST_n with DCKE[1:0] inputs LOW.
3. Disable RCD CKE Power Down mode in F0RC09-DA3 (disabled by default) and apply other basic RCD02 configuration settings such as F0RC0A (DIMM Operating Speed), F0RC0D (DIMM Configuration), F0RC0F (Command Latency Adder), and F0RC3x (Fine Granularity RDIMM Operating Speed).
4. While DRAMs of all ranks are in power down state, send 'Gear-down Mode Delay CS' command F0RC06 CMD 7 to register. This command will configure the register to delay the chip select for any command it receives by 1 nCK relative to the baseline command delay in F0RC0F. This ensures that the pair of MRS commands and NOP command that put the DRAMs into Gear-down Mode are received by the DRAM with the required setup time. This behavior remains in effect until the Register receives the 'Gear-down Mode Entry' command F0RC06 CMD 8 or Gear-down Mode exit CMD 10.

5. Assertion of CKE to enable the Rank, starting with Rank 0.
6. Memory controller sends low frequency ($t_{GEAR\_setup} + t_{GEAR\_hold}$)[1] MRS command to A-side of Rank 0 MR3 with A3=1, which will configure Gear-down Mode for the A-side DRAMs. This ensures that the RCD drives the A-side MRS command for a minimum total time of ($t_{GEAR\_setup} + t_{GEAR\_hold}$)1 cycles. Memory controller sends low frequency ($t_{GEAR\_setup} + t_{GEAR\_hold}$)1 MRS command to B-side of Rank 0 MR3 with A3=1, which will configure Gear-down Mode for the B-side DRAMs. The register must drive the B-side MRS command for a minimum total time of ($t_{GEAR\_setup} + t_{GEAR\_hold}$)1 cycles.
7. Memory controller sends 1N sync pulse with a low frequency ($t_{GEAR\_setup} + t_{GEAR\_hold}$)1 NOP command t_{SYNC_GEAR} clocks (even number) after the MRS command to Rank 0. This pulse is intended for the DRAMs and it will have no effect in the RCD. This ensures that the RCD drives the NOP command for a minimum total time of ($t_{GEAR\_setup} + t_{GEAR\_hold}$)1 cycles.
8. The host repeats steps 5 to 7 for all other Ranks on the DIMM and subsequent Gear-down entries must be on the same even clock boundary as Rank 0.
9. The host drives CKE LOW 4 clock cycles prior to 'Gear-down Mode Entry' CMD. This puts the DRAMs in power down state to prevent the DRAMs from getting invalid high-speed (one cycle) MRS command to MR7.
10. The memory controller sends a low frequency ($t_{GEAR\_setup} + t_{GEAR\_hold}$)1 'Gear-down Mode Entry' command F0RC06 CMD 8 with CKE LOW and the RCD enters Gear-down Mode.
11. The host can now drive CKE HIGH and Normal operation in 2N mode starts $t_{CMD\_RCD\_GEAR}$ clocks later. At this point the DRAMs and RCD are in Gear-down Mode. In Gear-down Mode, the register asserts the CA and CTRL outputs with the rising edge of the Y_t clock outputs (rather than with the falling edge). This guarantees that the DRAM sees an additional half tCK of setup time. The RCD will use the Gear-down Mode Entry command as the sync signal that will select the alignment of the internal divided clock that will be used to receive the CMD/ADD/CTRL signals at the input receivers. The RCD will forward a command to the QxCA outputs for every cycle a DCS_n input is registered LOW.
12. RCD CKE Power Down mode can now be enabled in F0RC09-DA3.

Figure 23 shows a simplified diagram for the expected input and output signals of DDR4RCD02 during the Control Gear-down Mode entry sequence.

After exit from a clock stop power down mode the RCD will exit CGM. This means Step 3 and Steps 5 to 12 need to be executed to put the DRAM and DDR4RCD02 back into 2N mode. The Data Buffer interface always runs at full speed. However, Control Gear-down Mode does affect the timing of BCOM[3:0], BODT and BCKE. The Data Buffer interface timing should align with the memory interface. Since the propagation delay from CK_t/CK_c to QC/A is increased by (1/2) tCK, and the DRAMs will sample the QCA signals (1/2) tCK later than the normal mode, the effective propagation delay from the input sampling phase of RCD to the input sampling phase of DRAMs is increased by a total of 1tCK. Accordingly, the DB interface signals BCOM[3:0], BODT and BCKE should be delayed by 1 tCK, so that the propagation delay from the input sampling phase of RCD to the input sampling phase of DB aligns with the propagation delay from RCD to DRAMs. This way, the training range (write leveling or read leveling) of DB is unchanged.

1. t_{GEAR_setup} and t_{GEAR_hold} are DDR4 SDRAM parameters defined in JESD79-4.

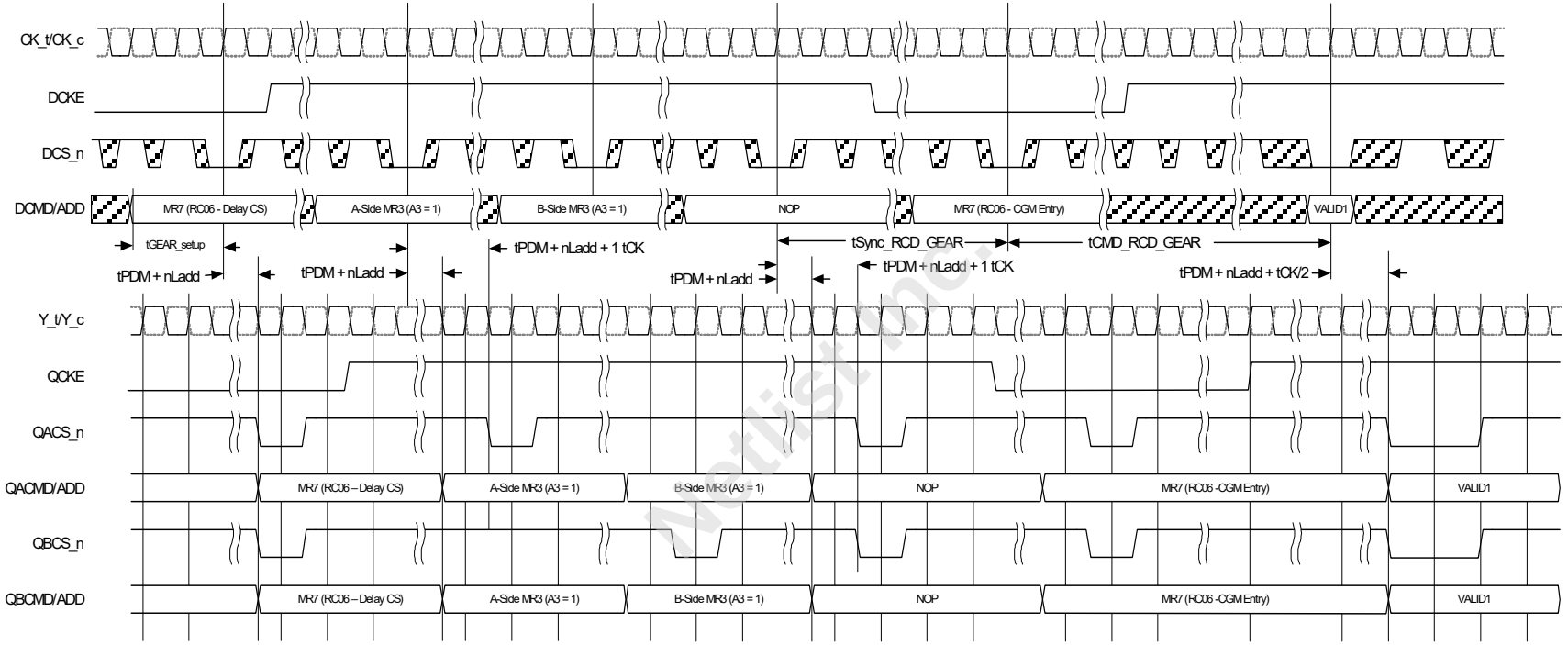


Figure 23 — Expected RCD input and output signals during Control Gear-down Mode entry sequence.

2.16.1 CKE Power Down Mode in Control Gear-down Mode

When Control Gear-down Mode is enabled, the tInDIS, tCKoff, tQDIS and tFixedoutput timing parameters must be adjusted to make them consistent with the fact that CA and CTRL signals are captured with a divided clock at the inputs of the RCD and the DRAMs. The Gear-down Mode specific values for these parameters are defined in Table 143, “Control Gear-down Mode Timing Parameters”.

2.16.2 Handling of parity errors in Control Gear-down Mode

Excepting for one difference in timing of the ALERT_n signal assertion, parity error handling is similar when Control Gear-down Mode is enabled or disabled. When CGM is enabled and a parity error is detected, ALERT_n is asserted four or six input clocks after the erroneous command is registered, depending on revision implementation. When CGM is disabled, this latency is only three clock cycles.

2.16.3 Output Delay Control Restrictions in Control Gear-down Mode

The fractional output delay features controlled by RCWs F1RC1x through F1RC9x are not supported when Control Gear-down Mode is enabled.

2.16.4 Weak Drive Feature in Control Gear-down Mode

Weak drive must be disabled during the Gear-down initialization sequence. The DDR4RCD02 device will automatically disable weak drive mode after it receives the F0RC06 CMD7 Gear-down CS Delay command, regardless of the setting in F0RC00 Bit DA1. After the F0RC06 CMD 8, Gear-down Entry command, weak drive mode will be enabled if F0RC00 Bit DA1 = 1 and QC/A outputs will go to weak drive whenever QxCS_n outputs are all HIGH.

2.17 Command to Address Latency (CAL) Mode

he DDR4RCD02 supports Command Address Latency (CAL) function as a power savings feature. tCAL is the delay in clock cycles between DCS[n[1]:0]_n assertion and DCA as defined in DRAM MR4 A8:A6 - see Table 15, “DRAM MRS settings for tCAL”. CAL Mode gives the DDR4RCD02 time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched, the receivers can be disabled again (see Figure 24). If weak drive is enabled, the RCD will drive the QxCA bus weak during tCAL.

As in regular mode, the DDR4RCD02 expects the DPAR input in the cycle after the other CMD/ADDR inputs (if parity checking is enabled) and the Command Latency Adder control word functionality is still available, with the delay adder counted from the sampling of the CMD/ADDR signals. In CAL Mode, the RCD always forwards DCS[x:0]_n inputs immediately to the QxCS[y:0]_n outputs (by using DC0 to decode the outputs when in encoded QuadCS mode) without adding the command latency adder. As a corollary, if a non-zero command latency adder is programmed in F0RC0F, the host delays the CMD/ADDR outputs relative to the assertion of DCS[y:0]_n by tCAL - command latency adder. This ensure that the DRAM sees the expected CAL latency adder without adding any unnecessary delay.

In CAL Mode, the RCD always forwards DCS[y:0]_n inputs to both QACS[y:0]_n and QBCS[y:0]_n outputs. When the RCD decodes a MRS command to the DRAM in CAL Mode, it uses DBGA1 or DBGA0 (used for mirrored ranks) to determine if the MRS command is to the A-side or the B-side and forwards the MRS command to the selected side and outputs a NOP command to the other side with the QCMD/QADD/QPAR outputs set to a condition which provides correct parity.

1. n=1 for direct DualCS and encoded QuadCS modes; n=3 for direct QuadCS mode

In Encoded QuadCS mode, the DDR4RCD02 captures DC0 with the DCSx_n LOW pulse since the host needs to send DC0 at the same time as the chip select so that the RCD can decode the chip select outputs. The host does not send DC0 again with the other CMD/ADDR signals.

The DCS[n[a]:0]_n and DC0 inputs remain always enabled in CAL Mode (unless they are statically disabled in disabled in F0RC08).

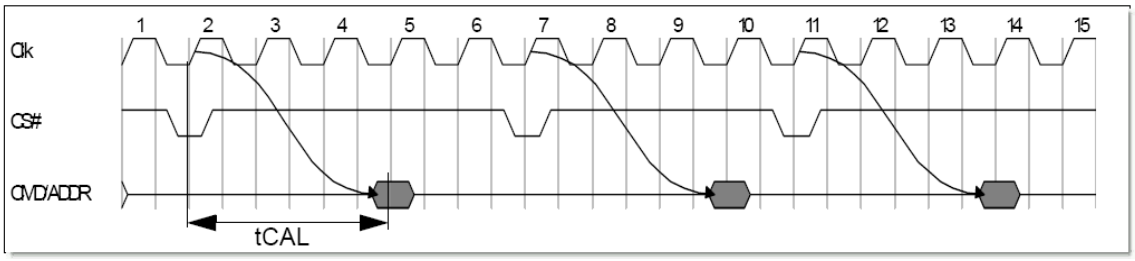


Figure 24 — Definition of CAL

Table 15 — DRAM MRS settings for tCAL

MR4 A[8:6]	tCAL [nCK]
000	Disabled (default)
001	3
010	4
011	5
100	6
101	8
110	Reserved
111	Reserved

Table 16 shows the DRAM timing requirements for tCAL at different data rates.

Table 16 — tCAL timing for different data rates

Data rate	tCAL [nCK]	tCAL [nCK] in Gear-down Mode
1600	3	4
1866	4	4
2133	4	4
2400	5	6
2667	5	6
2933	6	6
3200	6	6

Upon entry into CAL Mode (tCAL after a MRS command to MR4 A8:A6 that has any non-zero bits), all register input buffers are disabled except for CK_t/CK_c, DCS[n[1]:0]_n, DCKEn, DODTn and DRST_n.

For consecutive commands, the DDR4RCD02 will keep the DCA receivers enabled for the duration of tCAL,

measured from the previous command.

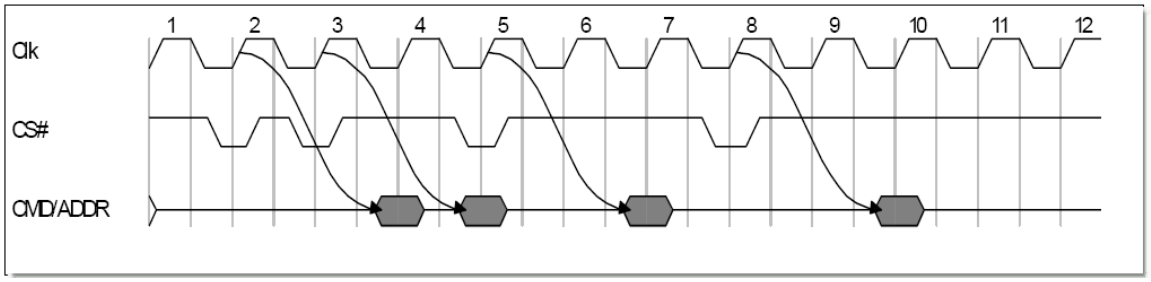


Figure 25 — CAL timing for consecutive commands

If CAL Mode snooping is enabled in F1RC01, the DDR4RCD02 will snoop the CA bus for MRS commands to Rank 0, A-side, to determine when the DIMM is put into CAL Mode and the tCAL latency value. Only during CAL Mode entry and exit when MR4[A8:A6] is a non-zero value, the host must first program MR4[A8:A6] (CS to CMD/ADDR Latency) in all DRAMs and sides other than Rank 0, A side. By programming Rank 0, A side last, the host will ensure DDR4 spec-compliant timing for all DRAMs during the CAL Mode entry sequence. The host must not mix any commands other than MRS to MR4 when programming DRAMs into CAL Mode. PDA access programming of MR4[A8:A6] to non-zero value on a subset of DRAMs is not supported.

In CAL Mode the RCD only checks parity in cycles following CMD/ADDR assertions, not in cycles when only DCS[x:0]_n is asserted. Following the detection of a CA parity error, the RCD outputs a NOP command on the QxCA outputs, while passing or blocking the remaining DCA and DPAR to QxCA and QxPAR, and then disables the QxCS[y:0] outputs **OR** continues driving a NOP command while passing through the remaining DCA and DPAR to QxCA and QxPAR until the end of the ALERT_n pulse or until a 'Clear CA parity error' command is received, depending on the setting in F0RC0E.

2.17.1 Handling of parity errors in CAL Mode

DDR4RCD02 needs to handle parity errors when CAL Mode is enabled. If a parity error occurs and parity checking is enabled in F0RC0E, the DDR4 register sets the 'CA Parity Error Status' bit in F0RCFx to '1' and disables parity checking. ALERT_n is asserted three input clocks after the erroneous command is registered. If the 'CA Parity Error Status' bit is '0', the DDR4 register logs the error by storing the erroneous command and address bits in the Error Log Register. ALERT_n stays asserted LOW until a 'Clear CA Parity Error Status' command is sent if the 'ALERT_n Assertion' bit in the Parity Control Word (F0RC0E) is '0'. In this case the erroneous command and all subsequent commands are forwarded as NOPs or DES to the DRAM until the memory controller issues 'Clear CA Parity Error' command, which will also clear the 'CA Parity Error Status' bit in the Error Log Register. If the 'ALERT_n Assertion' bit is '1', the ALERT_n pulse width is as defined in Table 39 with start of the ALERT_n pulse width counted from the third input clock edge after the 1st parity error. If the 'ALERT_n Re-enable' bit is '0', the erroneous command and all subsequent commands are forwarded as NOPs or DES to the DRAM until the end of the ALERT_n pulse width and parity checking remains disabled until a 'Clear CA Parity Error' command is sent, which will also clear the 'CA Parity Error Status' bit in the Error Log Register. If the 'ALERT_n Re-enable' bit is '1', the device will re-enable parity after the ALERT_n pulse and the device will forward commands to the DRAM. The 'CA Parity Error Status' bit will remain set. If a subsequent parity error is detected, the device will re-enter the parity error state and set the '> 1 Error' bit. The other bits in the Error Log Register are not updated on this subsequent error. Both the 'CA Parity Error Status' bit as well as the '> 1 Error' bit will be cleared by sending a 'Clear CA Parity Error' command.

2.18 Simultaneous CAL Mode and Control Gear-down Mode

CAL or CA parity mode must be disabled prior to a Gear-down command. They can be enabled again after tSYNC_RCD_GEAR and tCMD_RCD_GEAR periods are satisfied. Figure depicts a simple timing diagram example of the expected input and output signals when CAL node and Gear-down Mode are both enabled at the same time.

2.18.1 Clock-stopped power down events when CAL+CGM are enabled

CAL Mode must be disabled before CKOFF (clock-stop power down) event if CGM (Control Gear-down Mode) is enabled.

NOTE: This is necessary in order to support the sequence to enter Gear-down Mode after clock stopped power down exit.

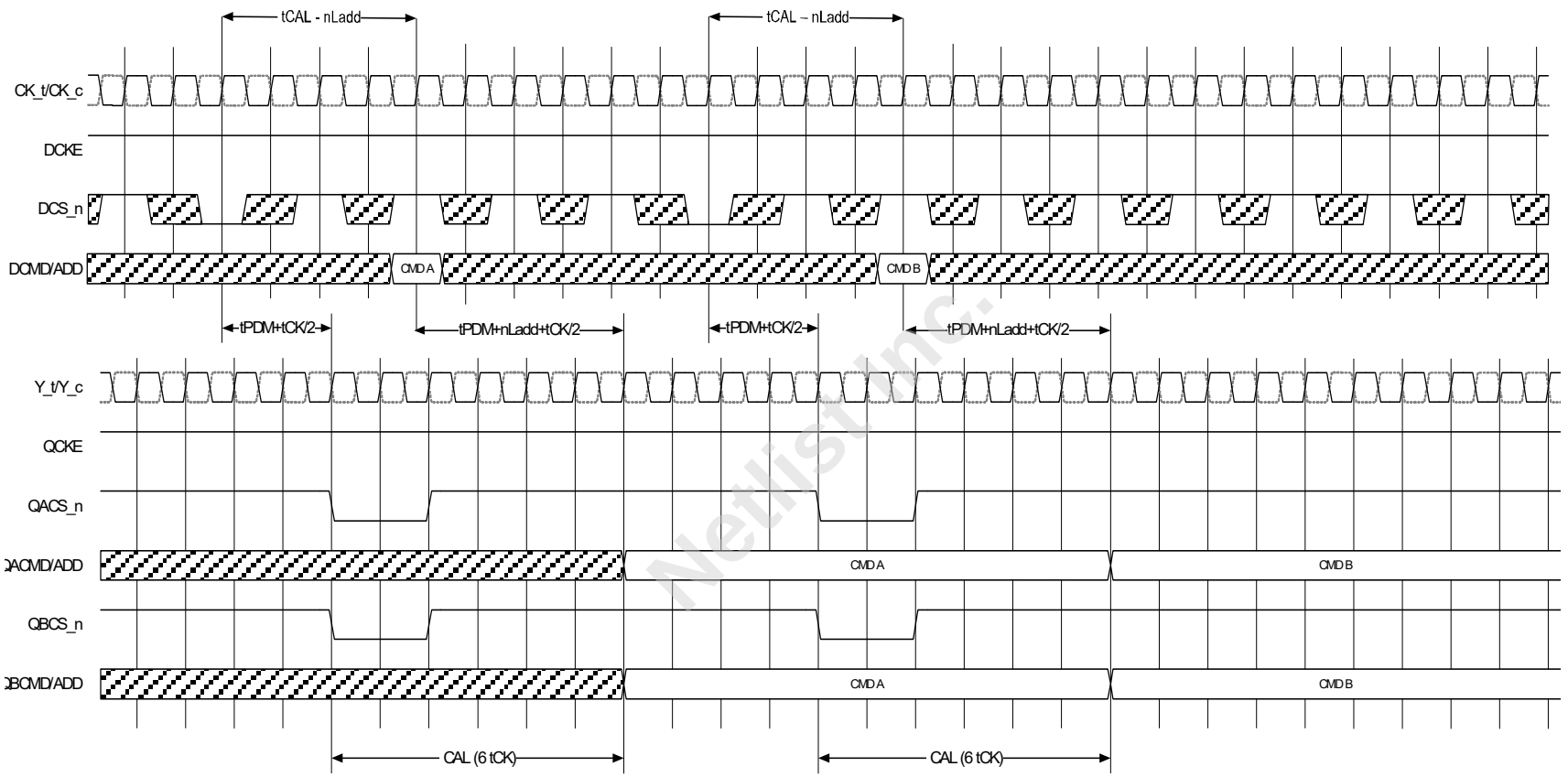


Figure 26 — Timing diagram example for a case with Control Gear-down Mode and CAL mode enabled at the same time (Latency adder setting [nLadd] = 2 tCK, tCAL = 6 tCK).

2.19 Optional NVDIMM Support Feature

2.19.1 NVDIMM Initialization Sequence

The recommended sequence for initializing an NVDIMM using the NV mode features of the DDR4 RCD02 and DB02 devices is shown below.

1. Power up.
   a. NV local controller starts with LCOM[2:0] and LCK_t/LCK_c pins disabled and LCKE pin driven LOW.
2. Check SPD.
3. Configure RCD02 and DB02 basic settings.
4. Execute DRAM initialization sequence.
5. Perform Host to RCD02/DB02/DRAM training sequences as needed.
6. Enable NVDIMM mode (Write F4RC00 – DA0 = 1).[1]
   a. LCOM[1:0] start driving static LOW (F4RC01 – DA[1:0]).
7. Host can lock NVDIMM mode enable by setting F0RC0E – DA1 = 1 before the lockout time is started in the NVDIMM (i.e., within t_{MRD_L2} = 32 t_{CK} from the RCW Write command that sets Bit DA0 in F4RC00 to 1).
8. The Host controller writes register MODULE_OPS_CONFIG-Offset 0xAA bit3 in the NV local controller (through I^2C) to enable monitoring of LCOM[1:0] asynchronous interrupt signal.
9. Wait lockout time (1 sec) for NVDIMM internal initialization.
   a. The lockout time window starts t_{MRD_L2} = 32 t_{CK} after the RCW Write command that sets Bit DA0 in F4RC00 to 1.
   b. NV local controller allowed to drive LCOM[2:0] and LCK_t/LCK_c.
   c. No activity allowed on DRAM channel during the lockout window.
   d. No activity is allowed on the I^2C bus during the lockout window excepting for the command in Step 8 above.
10. Initiate normal operation. The Host can arm the NVC at this point.

2.19.2 Save Mode Entry Sequence

The recommended sequence to enter Save Mode in an NVDIMM using the NV mode features of the DDR4 RCD02 and DB02 devices is shown below. According to the Byte Addressable Energy Backed Interface specification, Save operations can be initiated through the SAVE_n pin or through certain control register bits in the NV local controller. The sequence shown below applies to all Save operations regardless of the method used to initiate them.

1. Host puts DRAMs in Self Refresh.
2. RCD tracks DRAM Self Refresh state associated with DCKE0 and DCKE1 in F4RC6x.
   a. NV controller puts active DRAM ranks in Self Refresh.
3. NV local controller enables local clock LCK, masks platform clock and C/A signals (F4RC00 – DA[2:1] = 11b).
   a. NVDIMM settings configured previously (during Initialization).
4. NV local controller waits for RCD/DB clocks to stabilize (t_{STAB} + t_{DLLK}).
5. NV controller adjusts RCD02/DB02 (and DRAM) settings if needed.
6. NV local controller saves DRAM data in Non-Volatile Memory (only for ranks that were found in Self Refresh).

1. This step is performed by the combination of F0RC4x, F0RC5x and F0RC6x writes to execute CMD 5 CW Write Operation since the F0RC07 command features only apply to the LCOM[2:0] interface.

2.19.3 Save Mode Exit Sequence

The recommended sequence to exit Save Mode in an NVDIMM using the NV mode features of the DDR4 RCD02 and DB02 devices is shown below.

1. NV controller finishes saving DRAM data in Non-Volatile Memory.
2. NV controller restores RCD02/DB02 (and DRAM) settings it has modified (as needed).
3. NV controller puts active DRAMs in Self Refresh state.
4. NV controller gives RCD control back to the Host (F4RC00 – DA[2:1] = 00b).
5. NV controller drives LCKE Low and disables LCK_t/LCK_c and LCOM[2:0] drivers.

2.19.4 Restore Mode Entry Sequence

The recommended sequence to enter Restore Mode in an NVDIMM using the NV mode features of the DDR4 RCD02 and DB02 devices is shown below.

1. Host controller and NV local controller complete Steps 1 through 8 of Initialization Sequence.
   a. Optional period of normal operation (i.e., Restore operation can be requested by Host controller at any time and not always immediately after Initialization).
2. Host controller checks for presence of valid image.
3. If valid image is present Host controller requests Restore operation.
   a. NV controller assumes there is no valid data in DRAMs needing to be preserved.
   b. The Host shall not toggle DCKEn signal logic levels during the following three steps of this sequence.
   c. NV controller enables local clock LCK, masks platform clock and C/A signals (F4RC00 – DA[2:1] = 11b).
      1. NVDIMM settings configured previously (during Initialization).
   d. NV local controller waits for RCD/DB clocks to stabilize (t_{STAB} + t_{DLLK}).
   e. NV controller adjusts RCD02/DB02 (and DRAM) settings if needed.
   f. NV local controller restores data from non-volatile memory to DRAMs.

2.19.5 Restore Mode Exit Sequence

The recommended sequence to exit Restore Mode in an NVDIMM using the NV mode features of the DDR4 RCD02 and DB02 devices is shown below.

1. NV controller finishes restoring data from non-volatile memory to DRAMs.
2. NV controller restores RCD02/DB02 (and DRAM) settings it has modified (as needed).
3. NV controller puts active DRAMs in Self Refresh state.
4. NV controller disables local clock LCK, enables platform clock and C/A signals in RCD02 (F4RC00 – DA[2:1] = 00b).
   a. Host controller required to drive DCKEn signals Low at this time.
5. NV controller drives LCKE Low and disables LCK_t/LCK_c and LCOM[2:0] drivers.
6. Host controller initiates Erase procedure.
7. The Host controller is allowed to start normal operation.
   a. The Host can arm the NVC after meeting the maximum erase time specified in NVC registers.

2.19.6 LCOM[2:0] Command Frames

If the optional NVDIMM mode feature is supported, the LCOM[2:0] interface is available in the RCD02 and it can be used to receive command frames. Each command frame is driven from the NVDIMM local controller (NVC) to the RCD02 on the LCOM[2:0] interface and it contains all the CTRL/CMD/ADD signals of the Host interface with the exception of DPAR. Command frames are transferred sequentially using 16 LCK clock cycles as a packet. Table 17 below depicts the 16-cycle command frame in the LCOM[2:0] interface.

Table 17 — LCOM[2:0] Command Frame Definition

Time (clock cycle)	LCKE	LCOM2	LCOM1	LCOM0
0	1	Previous Command		
1	1	1	CKE0	CKE1
2	1	0	CS0_n	CS1_n
3	1	0	C0/CS2_n	C1/CS3_n
4	1	0	ODT0	ODT1
5	1	0	C2	ACT
6	1	0	A16/RAS_n	A15/CAS_n
7	1	0	A14/WE_n	BA0
8	1	0	BA1	BG0
9	1	0	BG1	A17
10	1	0	A13	A12
11	1	0	A11	A10
12	1	0	A9	A8
13	1	0	A7	A6
14	1	0	A5	A4
15	1	0	A3	A2
16	1	0	A1	A0

The purpose of the LCOM[2:0] interface is to allow the NVC to take over control of the RCD02 from the system Host controller. Therefore, the signals sent over this serialized interface are intended to update the corresponding CTRL/CMD/ADD outputs of the RCD02. When this feature is enabled, the RCD02 is required to execute all the commands it would execute if the same signals were coming from the conventional Host interface CTRL/CMD/ADD inputs. That includes, for example, RCW Writes and Data Buffer/DRAM Read and Write commands. One difference, however, is that the LCOM[2:0] interface can only provide one new command, or CTRL/CMD/ADD output signal state update, every 16 cycles of the LCK_t/LCK_c clock. The RCD02 will handle this by assuming that the input signals will be held constant during the 16 clock cycles until the next complete command frame has been received at the LCOM[2:0] interface. One notable exception to this are the chip select signals. Any chip select signals asserted LOW in a given command frame, will be treated as driven LOW for one clock cycle only. The RCD02 will use standard (JEDEC-defined) control words to determine if the C0/CS2_n and the C1/CS3_n LCOM[2:0] command bits need to be treated as Chip ID bits or as Chip Select signals.

2.19.7 LCOM[1:0] Read Data Frames

If the optional NVDIMM mode feature is supported, the LCOM[2:0] interface is available in the RCD02 and it can be used to send read data. Each read data frame is driven from the RCD02 to the NVC on the LCOM[2:0] interface contains 32 bits of internal RCD02 control word (RCW) data. If Bits DA1 or DA2 in F4RC00 are set to 1, RCW data selected in F0RC2x - DA5, F0RC4x, and F0RC6x - DA[7:4] are transferred sequentially using 32 LCK_t/LCK_c clock cycles as a packet. If F4RC00 - DA[2:1] = ‘00’, designated control word bytes F4RC1x .. F4RC4x are transferred sequentially using 32 LCK_t/LCK_c clock cycles as a packet. Table 18 below depicts the 32-cycle read data frame in the LCOM[2:0] interface. There is a latency of 4 tLCK cycles from the LCOM2 pulse to the start of the read data frame. Read data transfer occurs at a rate of 1, 2, or 4 tLCK per data bit (programmable in F4RC02 - DA[1:0]) to simplify NVDIMM local controller operation.

Table 18 — LCOM[2:0] Read Data Frame Definition
(Gear Ratio = 2 Selected in F4RC02 - DA[1:0])

Time (clock cycle)	LCKE	LCOM2	LCOM1	LCOM0
0	1	Previous Transfer or Idle		
1	1	1	F0RC07 CMD 4 Command Frame	
2	1	0		
...				
16	1	0		
17	1	0	Idle Cycles NVC Allowed to Drive LCOM[1:0] RCD02 NOT allowed to drive LCOM[1:0]	
18	1	0		
...				
24	1	0		
25	1	0	Idle Cycles RCD02 Allowed to Drive LCOM[1:0] with data from F4RC01 - DA[1:0] NVC NOT allowed to drive LCOM[1:0]	
26	1	0		
...				
32	1	0		
33	1	1	F4RC01 - DA1	F4RC01 - DA0
34	1	0		
35	1	0		
36	1	0		
37	1	0	Bit 1, 1st CW Byte	Bit 0, 1st CW Byte
38	1	0		
39	1	0	Bit 3, 1st CW Byte	Bit 2, 1st CW Byte
40	1	0		
...				
65	1	0	Bit 5, 4th CW Byte	Bit 4, 4th CW Byte
66	1			
67	1	0	Bit 7, 4th CW Byte	Bit 6, 4th CW Byte
68	1			
69	1	0	Idle Cycles RCD02 Allowed to Drive LCOM[1:0] with data from F4RC01 - DA[1:0]	
70	1	0		
...				
76	1	0		
77	1	0	Idle Cycles NVC Allowed to Drive LCOM[1:0]	
78	1	0		
...				
84	1	0		
85	1	NVC Allowed to Start New Command Frame (from NVC to RCD02)		

To initiate a read data transfer, the NVC must first send an RCW Read command (F0RC07 CMD 4) to the RCD02 through the LCOM[2:0] interface. After receiving F0RC07 CMD 4, the RCD02 will wait for at least tMRD (8 LCK clock cycles) before starting to drive the LCOM[1:0] lines as outputs. The NVC is required to stop driving the LCOM[1:0] lines by the time tMRD time expires. After sending F0RC07 CMD 4, the NVC is required to wait for at least tMRC (16 LCK clock cycles) before requesting start of the data frame transfer by pulsing LCOM2 HIGH for one LCK clock cycle. Note that in this case tMRD and tMRC are measured from the end of the command frame containing F0RC07 CMD 4. After completing the data frame transfer, the RCD02 is required to stop driving the LCOM[1:0] lines within tMRD time (8 LCK clock cycles). The NVC is required to wait for at least tMRC (16 LCK clock cycles) time before it starts driving the LCOM[1:0] signals and sending the first LCOM2 pulse corresponding to a new command frame. Summarizing, a single read data transfer takes a minimum of 84 LCK clock cycles (16 + tMRC + 36 + tMRC = 16 + 36 + 32) when Gear Ratio = 2 is selected in F4RC02 - DA[1:0]. Table 19 defines the addressing scheme for control word read access in LCOM[2:0] read data frames initiated through F0RC07 CMD 4 when the Host command interface is disabled (i.e., when F4RC00 - DA[2:1] are not set to '00').

.

Table 19 — Read Data Frame Target RCW Selection

F0RC4x - DA[3:0]				F0RC6x - DA[7:4]				Target RCW Byte			
								1st Byte	2nd Byte	3rd Byte	4th Byte
0	0	0	0	0	x	x	x	{FnRC01, FnRC00}[1]	{FnRC03, FnRC02}[1]	{FnRC05, FnRC04}[1]	{FnRC07, FnRC06}[1]
0	0	0	0	1	x	x	x	{FnRC09, FnRC08}[1]	{FnRC0B, FnRC0A}[1]	{FnRC0D, FnRC0C}[1]	{FnRC0F, FnRC0E}[1]
0	0	0	1	x	x	x	x	FnRC1x[1]	FnRC2x[1]	FnRC3x[1]	FnRC4x[1]
0	0	1	0	x	x	x	x				
0	0	1	1	x	x	x	x				
0	1	0	0	x	x	x	x				
0	1	0	1	x	x	x	x	FnRC5x[1]	FnRC6x[1]	FnRC7x[1]	FnRC8x[1]
0	1	1	0	x	x	x	x				
0	1	1	1	x	x	x	x				
1	0	0	0	x	x	x	x				
1	0	0	1	x	x	x	x	FnRC9x[1]	FnRCAx[1]	FnRCBx[1]	FnRCCx[1]
1	0	1	0	x	x	x	x				
1	0	1	1	x	x	x	x				
1	1	0	0	x	x	x	x				
1	1	0	1	x	x	x	x	FnRCDx[1]	FnRCEx[1]	FnRCFx[1]	0000_0000
1	1	1	0	x	x	x	x				
1	1	1	1	x	x	x	x				

1. Function space 'Fn' is selected by Bits DA[7:5] in F0RC4x and Bit DA5 in F0RC2x.

2.19.8 LCOM[1:0] Asynchronous Interrupt Feature

If the optional NVDIMM mode feature is supported, the LCOM[2:0] interface is available in the RCD02 and it can be used to send asynchronous interrupt signals. If input LCKE is driven LOW by the NVDIMM local controller, the LCOM[1:0] signals are driven statically by the RCD02 with logic levels corresponding to the settings stored in F4RC01 - DA[1:0]. These control word bits can be used to signal asynchronous interrupt events to the NVC. These interrupt events can be controlled directly by the Host controller or by internal RCD02 hardware by updating the settings contained in F4RC01 - DA[1:0]. Similarly, the NVDIMM local controller can update the values of these control word bits to clear the interrupt event signal if needed.

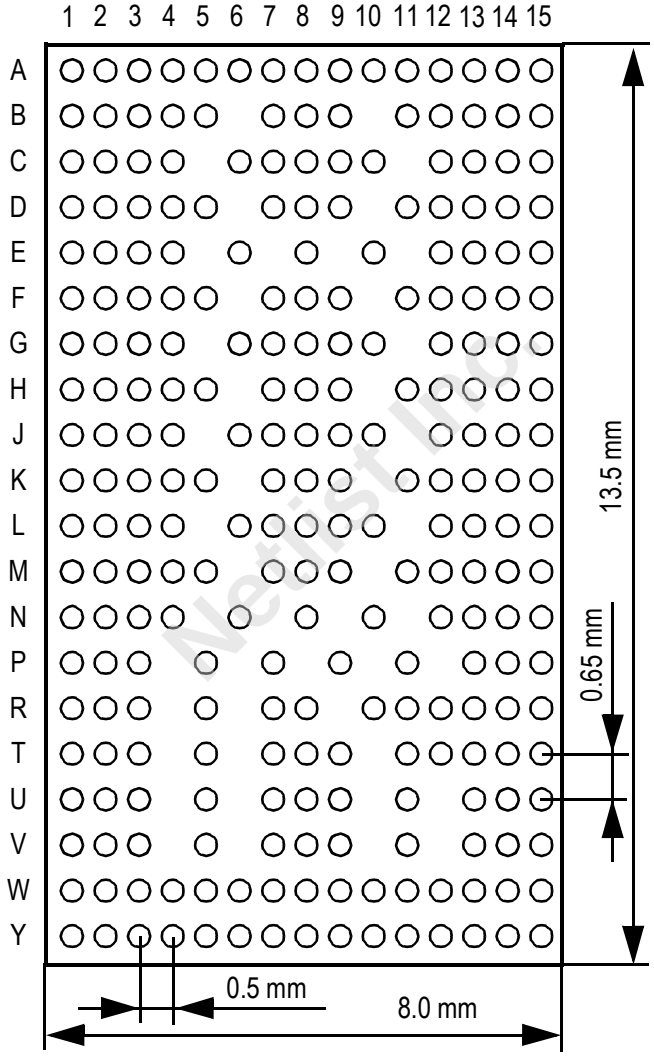
NOTE: It is not necessary for the LCK_t/LCK_c clock signal to be running when LCKE is driven LOW.

2.19.9 Control Word Access Protection

When F4RC00 - DA[2:0] = '001', the LCOM[2:0] interface is allowed to issue Control Word Write commands. At this time the Host interface inputs are also enabled and they can be used to issue RCW Read and Write commands. To avoid conflicts in this case (i.e., F4RC00 - DA[2:0] = '001') the RCD02 hardware will allow RCW Write access through the LCOM[2:0] interface to Control Word locations F0RC07, F4RC00, and F4RC02, exclusively. The RCD02 will only allow RCW Read access through the LCOM[2:0] interface to Control Words F4RC1x .. F4RC4x in this case. At the same time, Control Words F0RC07, F4RC00, and F4RC02 will not be accessible for Writes or Reads through the Host CTRL/CMD/ADD or I2C interfaces (i.e., they will be treated as reserved locations).Finally, Read access will not be allowed for Control Words F4RC1x .. F4RC4x through the Host CTRL/CMD/ADD or I2C interfaces in this case. If NVDIMM mode is enabled, the LCOM[2:0] interface will have unrestricted access to all control words in the RCD02 only when the LCK_t/LCK_c Input Clock Selection control bit (F4RC00 - DA1) is set to 1 or when the Host CTRL/CMD/ADD Interface Selection control bit (F4RC00 - DA2) is set to 1.

2.20 Mechanical outline

Package options include a 253-ball Flip-Chip Fine-Pitch BGA (FCBGA) with 0.5 mm/0.65 mm ball pitch, 15 x 20 grid with 47 balls depopulated, 8.0 mm x 13.5 mm as defined in MO-307A. The device pinout supports outputs on the outer left and right columns to support easy DIMM signal routing. Corresponding inputs are placed in a way to match the corresponding pin location on the connector. Each input and output is located close to an associated no ball position or on the outer two rows to allow low cost via technology combined with the small 0.5 mm/0.65 mm ball pitch.



Ball diameter: 0.30 mm

Ball pitch: 0.5 mm x 0.65 mm

Figure 27 — Ball Configuration

2.21 Pinout

Table 20 specifies the pinout for the DDR4RCD02 including optional pin functions to support NVDIMM[1]. The device has (mostly) symmetric pinout with inputs at the south side and outputs to east and west sides.

Table 20 — Ball Assignment - 253-ball FCBGA, 15 x 20 Grid, TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	NU	QAPAR	QAA17	QAA13	QAA11	QAA8	RFU0	ZQCAL	RFU1	QBA8	QBA11	QBA13	QBA17	QBPAR	NU
B	QAA9	QAA2	V_{SS}	V_{SS}	QAA7		V_{DD}	V_{DD}	V_{DD}		QBA7	V_{SS}	V_{SS}	QBA2	QBA9
C	QAA0	V_{DD}	V_{DD}	QAA5		V_{SS}	V_{SS}	V_{DD}	V_{SS}	V_{SS}		QBA5	V_{DD}	V_{DD}	QBA0
D	QAA1	QAA6	V_{SS}	V_{SS}	QAA3		V_{DD}	V_{DD}	V_{DD}		QBA3	V_{SS}	V_{SS}	QBA6	QBA1
E	QAA10	V_{DD}	V_{DD}	QABG0		QABA1		V_{DD}		QBBA1		QBBG0	V_{DD}	V_{DD}	QBA10
F	QAA4	QABA0	V_{SS}	V_{SS}	QABG1		V_{SS}	V_{SS}	V_{SS}		QBBG1	VSS	V_{SS}	QBBA0	QBA4
G	QAA12	V_{DD}	V_{DD}	QAC0/CS2_n		V_{DD}	V_{DD}	V_{SS}	V_{DD}	V_{DD}		QBC0/CS2_n	V_{DD}	V_{DD}	QBA12
H	QAA14/WE_n	QAA16/RAS_n	V_{SS}	V_{SS}	QACKE0		V_{SS}	V_{SS}	V_{SS}		QBCKE0	V_{SS}	V_{SS}	QBA16/RAS_n	QBA14/WE_n
J	QAACT_n	V_{DD}	V_{DD}	QAC1/CS3_n		V_{DD}	V_{DD}	V_{SS}	V_{DD}	V_{DD}		QBC1/CS3_n	V_{DD}	V_{DD}	QBAC-T_n
K	QAA15/CAS_n	QACS0_n	V_{SS}	V_{SS}	QACS1_n		V_{SS}	V_{SS}	V_{SS}		QBCS1_n	V_{SS}	V_{SS}	QBCS0_n	QBA15/CAS_n
L	QACKE1	V_{DD}	V_{DD}	QAODT1		V_{DD}	V_{DD}	V_{SS}	V_{DD}	V_{DD}		QBODT1	V_{DD}	V_{DD}	QBCKE1
M	QAC2	QAODT0	V_{SS}	V_{SS}	ALERT_n		V_{SS}	V_{SS}	V_{SS}		QRST_n	V_{SS}	V_{SS}	QBODT0	QBC2
N	RFU2, LCKE	SA2	V_{DD}	BCOM3		BCKE		BCOM1		BVrefCA		V_{DDSPD}	V_{DD}	SCL	SDA
P	DRST_n	ERROR_IN_n	V_{DD}		BCK_t		BCOM0		SA0		BCOM2		V_{DD}	DC1/CS3_n	DC0/CS2_n
R	DCKE1	DCKE0	V_{SS}		BCK_c		QVrefCA	PV_{SS}		VrefCA	AV_{DD}	AV_{DD}	V_{SS}	DA13	DA17
T	DACT_n	DBG0	V_{SS}		RFU3, LCOM2		BODT	PV_{SS}	SA1		AV_{SS}	AV_{SS}	V_{SS}	DODT1, NC	DC2, NC
U	DA11	DA12	V_{DD}		Y1_t		Y3_t, LCK_t	PV_{DD}	Y2_t, LCOM1		Y0_t		V_{DD}	DCS1_n	DA14/WE_n
V	DA9	DBG1	V_{DD}		Y1_c		Y3_c, LCK_c	PV_{DD}	Y2_c, LCOM0		Y0_c		V_{DD}	DA15/CAS_n	DODT0, NC
W	DA7	DA8	V_{SS}	V_{SS}	V_{DD}	V_{DD}	BFUNC	V_{SS}	V_{SS}	V_{DD}	V_{DD}	V_{SS}	V_{SS}	DA16/RAS_n	DCS0_n
Y	NU	DA5	DA6	DA4	DA3	DA1	DA2	CK_t	CK_c	DPAR	DA0	DBA1	DBA0	DA10	NU

1. NVDIMM features are not mandatory in DDR4RCD02

2.21.1 Terminal Functions Function tables

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
Input Control bus	DCKE0/1 DODT0/1	CMOS[1] V_{REF} based	DRAM corresponding register function pins not associated with Chip Select.
	DCS0_n..DCS1_n	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals.
	DCS2_n..DCS3_n or DC0..DC1	CMOS[1] V_{REF} based	DRAM corresponding register Chip Select signals. These pins initiate DRAM address/command decodes,. Some of these have alternative functions: • DCS2_n <=> DC0 • DCS3_n <=> DC1
	DC2	CMOS[1] V_{REF} based	DRAM corresponding register Chip ID 2 signal.
Input Address and Command bus	DA0..DA13, DA17 DBA0..DBA1, DBG0..DBG1	CMOS[1] V_{REF} based	DRAM corresponding register inputs.
	DA14..DA16 or DWE_n, DCAS_n, DRAS_n	CMOS[1] V_{REF} based	DRAM corresponding register inputs. In case of an ACT command some of these terminals have an alternative function: DRAM corresponding register command signals. • DA14 <=> DWE_n • DA15 <=> DCAS_n • DA16 <=> DRAS_n
	DACT_n	CMOS[1] V_{REF} based	DRAM corresponding register DACT_n signal.
Clock inputs	CK_t/CK_c	CMOS differential	Differential master clock input pair to the PLL with a 10 KΩ ~ 100 KΩ pull-down resistor.
Reset input	DRST_n	CMOS input	Active LOW asynchronous reset input. When LOW, it causes a reset of the internal latches and disables the outputs, thereby forcing the outputs to float.
Parity input	DPAR	CMOS[1] V_{REF} based	Input parity is received on pin DPAR and should maintain even parity across the address and command inputs (see above), at the rising edge of the input clock.
Error input	ERROR_IN_n	Low voltage swing CMOS input	DRAM address parity and CRC ALERT_n output is connected to this input pin, which in turn is buffered and redriven to the ALERT_n output of the register. Requires external pull up resistor. In LRDIMM applications, the DB ALERT_n outputs are also connected to this input.
Data buffer control and communication outputs	BODT	CMOS[2]	Data buffer on-die termination signal
	BCKE	CMOS[2]	Data buffer clock enable signal for PLL power management
	BCOM[3:0]	CMOS[2]	Register communication bus for data buffer programming and control access
	BCK_t/BCK_c	CMOS[2] differential	Differential clock output pair to the data buffer.
	BVrefCA	$V_{DD}/2$	Output reference voltage for data buffer control bus receivers

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
Output Control bus	QACKE0/1, QAODT0/1, QBCKE0/1, QBODT0/1	CMOS[2]	Register output CKE and ODT signals.
	QACS0_n..QACS1_n, QBCS0_n..QBCS1_n	CMOS[2]	Register output Chip Select signals.
	QACS2_n..QACS3_n, QBCS2_n..QBCS3_n or QAC0..QAC1, QBC0..QBC1	CMOS[2]	Register output Chip Select signals. These pins initiate DRAM address/command decodes. Some of these have alternative functions: • QxCS2_n <=> QxC0 • QxCS3_n <=> QxC1
	QAC2, QBC2	CMOS[2]	Register output Chip ID2 signals.
Output Address and Command bus	QAA0..QAA13, QAA17, QBA0..QBA13, QBA17, QABA0..QABA1, QBBA0..QBBA1, QAG0..QAG1, QBG0..QBG1	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
	QAA14..QAA16, QBA14..QBA16 or QAWE_n, QACAS_n, QARAS_n, QBWE_n, QBCAS_n, QBRAS_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock. In case of an ACT command some of these terminals have an alternative function: Register output command signals. • QxA14 <=> QxWE_n • QxA15 <=> QxCAS_n • QxA16 <=> QxRAS_n
	QAACT_n, QBACT_n	CMOS[2]	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Vref output	QVrefCA	$V_{DD}/2$	Output reference voltage for DRAM receivers
Clock outputs	Y0_t..Y3_t, Y0_c..Y3_c or Y0_t, Y1_t, LCOM1, LCK_t Y0_c, Y1_c, LCOM0, LCK_c	CMOS[2] differential	Redriven clock for RDIMM and LRDIMM These pins have alternative functions for optional NVDIMM support. • Y2_t <=> LCOM1 (bidirectional pin) • Y2_c <=> LCOM0 (bidirectional pin) • Y3_t <=> LCK_t (input pin) • Y3_c <=> LCK_c (input pin)
RFU2	RFU2 or LCKE	CMOS[2]	Reserved for RDIMM and LRDIMM This pins has an alternative fuction for optional NVDIMM support. • RFU2 <=> LCKE (input pin)
RFU3	RFU3 or LCOM2	CMOS[2]	Reserved for RDIMM and LRDIMM This pins has an alternative function for optional NVDIMM support. • RFU3 <=> LCOM2 (input pin)
Reset output	QRST_n	CMOS[2]	Redriven reset. This is an asynchronous output. It is the responsibility of the DDR4RCD02 QRST_n to reset the DDR4 SDRAM on all DIMM topologies.
Parity outputs	QAPAR QBPAR	CMOS[2]	Redriven parity[3]
Error out	ALERT_n	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs when parity checking is enabled or that the ERROR_IN_n input was asserted, regardless of whether parity checking is enabled or not.

Table 21 — Terminal functions

Signal Group	Signal Name	Type	Description
I^2C Bus pins	SDA	Open drain I/O	I^2C Bus Data
	SCL	CMOS input[4]	I^2C Bus Clock
	SA[2:0]	CMOS input[4]	I^2C Bus Address signals
	BFUNC	CMOS input[5]	Function pin. BFUNC=V_{SS} for primary register, BFUNC=V_{DD} for secondary register
	V_{DDSPD}	Power input	I^2C Bus power input
Miscellaneous pins	VrefCA	$V_{DD}/2$	Input reference voltage for the CMOS inputs.
	V_{DD}	Power Input	Power supply voltage
	V_{SS}	Ground Input	Ground
	AV_{DD}	Analog Power	Analog supply voltage
	AV_{SS}	Analog Ground	Analog ground
	PV_{DD}	Clock Driver Output Power	Clock logic and clock output driver power supply
	PV_{SS}	Clock Driver Output Ground	Clock logic and clock output driver ground
	ZQCAL	Reference	Reference pin for driver calibration
	NU	Mechanical ball	Do not connect on PCB
	RFU[3:0]	I/O	Reserved for future use pins, must be left floating on DIMM and in DDR4RCD02

1. These receivers use internal or external VrefCA as the switching point reference.
2. These outputs with rail to rail signal swing and programmable impedance are optimized for memory applications to drive DRAM inputs over a terminated transmission line.
3. QBPAR will be inverted relative to DPAR if the device is configured with a parity calculation field = 00 in the Parity Control Word.
4. These inputs are 2.5 V inputs
5. This input is a 1.2 V input

Table 22 — Direct DualCS mode Function table (CS mode setting '00')

Inputs					Outputs				
DRST_n	DCS[1:0]_n[1]	CK_t[2]	CK_c[1]	CA[3]	Qn[4]	QxC[2:0]	QxCS[1:0]_n	QxODTn[5]	QxCKEn
H	XX	L or H	H or L	X	No change	No change	No change	No change	No change
H	LH	↑	↓	Dn	Dn	DC[2:0]	LH	DODTn	DCKEn
H	HL	↑	↓	Dn	Dn	DC[2:0]	HL	DODTn	DCKEn
H	LL	↑	↓	Dn	Dn	DC[2:0]	LL	DODTn	DCKEn
H	XX	L	L	X	float	float	float	float	L
H	HH	↑	↓	X	No change or float[6]	No change or float[6]	HH	DODTn	DCKEn
L	X or float	X or float	X or float	X or float	float	float	float	float	L

1. Only one DCSx_n input can the asserted for DRAM MRS and read commands.
2. It is illegal to hold both the CK_t and CK_c inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when DRST_n is driven HIGH.
3. CA = DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DODT0..DODT1, DCKE0..DCKE1, DC[2:0]
4. Qn = QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2
5. This column only applies when RC8x, DA7 = 0, otherwise the QxODTn outputs are not directly controlled by the DODTn inputs.
6. Depending on the power down modes activated.

Table 23 — Direct QuadCS mode Function table (CS mode setting '01')

Inputs					Outputs			
DRST_n	DCS[3:0]_n[1]	CK_t[2]	CK_c	CA[3]	Qn[4]	QxCS[3:0]_n	QxODTn[5]	QxCKEn
H	XXXX	L or H	H or L	X	No change	No change	No change	No change
H	HHHL	↑	↓	Dn	Dn	HHHL	DODTn	DCKEn
H	HHLH	↑	↓	Dn	Dn	HHLH	DODTn	DCKEn
H	HHLL	↑	↓	Dn	Dn	HHLL	DODTn	DCKEn
H	HLHH	↑	↓	Dn	Dn	HLHH	DODTn	DCKEn
H	HLHL	↑	↓	Dn	Dn	HLHL	DODTn	DCKEn
H	HLLH	↑	↓	Dn	Dn	HLLH	DODTn	DCKEn
H	HLLL	↑	↓	Dn	Dn	HLLL	DODTn	DCKEn
H	LHHH	↑	↓	Dn	Dn	LHHH	DODTn	DCKEn
H	LHHL	↑	↓	Dn	Dn	LHHL	DODTn	DCKEn
H	LHLH	↑	↓	Dn	Dn	LHLH	DODTn	DCKEn
H	LHLL	↑	↓	Dn	Dn	LHLL	DODTn	DCKEn
H	LLHH	↑	↓	Dn	Dn	LLHH	DODTn	DCKEn
H	LLHL	↑	↓	Dn	Dn	LLHL	DODTn	DCKEn
H	LLLH	↑	↓	Dn	Dn	LLLH	DODTn	DCKEn
H	LLLL	↑	↓	Dn	Dn	LLLL	DODTn	DCKEn
H	XXXX	L	L	X	float	float	float	L
H	HHHH	↑	↓	X	No change or float[6]	HHHH	DODTn	DCKEn
L	X or float	X or float	X or float	X or float	float	float	float	L

1. Only one DCSx_n input can the asserted for DRAM MRS and read commands.
2. It is illegal to hold both the CK_t and CK_c inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when DRST_n is driven HIGH.
3. CA = DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DODT0..DODT1, DCKE0..DCKE1, DC2
4. Qn = QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2
5. This column only applies when RC8x, DA7 = 0, otherwise the QxODTn outputs are not directly controlled by the DODTn inputs.
6. Depending on the power down modes activated.

Table 24 — Encoded QuadCS mode Function table (CS mode setting '11')

Inputs						Outputs			
DRST_n	DCS[1:0]_n[1]	DC0	CK_t[2]	CK_c[1]	CA[3]	Qn[4]	QxCS[3:0]_n	QxODT[5]n	QxCKEn
H	XX	X	L or H	H or L	X	No change	No change	No change	No change
H	HL	L	↑	↓	Dn	Dn	HHHL	DODTn	DCKEn
H		H	↑	↓	Dn	Dn	HHLH	DODTn	DCKEn
H	LH	L	↑	↓	Dn	Dn	HLHH	DODTn	DCKEn
H		H	↑	↓	Dn	Dn	LHHH	DODTn	DCKEn
H	LL	L	↑	↓	Dn	Dn	HLHL	DODTn	DCKEn
H		H	↑	↓	Dn	Dn	LHLH	DODTn	DCKEn
H	XX	X	L	L	X	float	float	float	L
H	HH	X	↑	↓	X	No change or float[6]	HHHH	DODTn	DCKEn
L	X or float	X or float	X or float	X or float	X or float	float	float	float	L

1. Only one DCSx_n input can the asserted for DRAM MRS and read commands.
2. It is illegal to hold both the CK_t and CK_c inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when DRST_n is driven HIGH.
3. CA = DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DODT0..DODT1, DCKE0..DCKE1, ,DC2
4. Qn = QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2
5. This column only applies when F0RC8x, DA7 = 0, otherwise the QxODTn outputs are not directly controlled by the DODTn inputs.
6. Depending on the power down modes activated.

Table 25 — PLL function table

Inputs					Outputs		
DRST_n	**AV_{DD}**	**OEn[1]**	**CK_t[2]**	**CK_c[2]**	**Yn_t**	**Yn_c**	**PLL**
L	X	X	X	X	Float	Float	Off
H	V_{DD} nominal	L	L	H	L	H	On
H	V_{DD} nominal	L	H	L	H	L	On
H	V_{DD} nominal	H	L	H	Float	Float	On
H	V_{DD} nominal	H	H	L	Float	Float	On
H	V_{DD} nominal	X	L	L	Float	Float	Off
H	V_{SS}[3]	L	L	H	L	H	Bypass/Off
H	V_{SS3}	L	H	L	H	L	Bypass/Off
H	V_{SS}	H	L	H	Float	Float	Bypass/Off
H	V_{SS}	H	H	L	Float	Float	Bypass/Off
H	V_{SS}	X	L	L	Float	Float	Bypass/Off
H	X	X	H	H	Reserved		

1. The Output Enable (OEn) to disable the output buffer is not an input signal to the DDR4RCD02, but an internal signal from the PLL powerdown control and test logic. It is controlled by setting or clearing the corresponding bit in the Clock Driver Enable control word.
2. It is illegal to hold both the CK_t and CK_c inputs at static logic HIGH levels or static complementary logic levels (LOW and HIGH) when DRST_n is driven HIGH.
3. This is a device test mode and all register timing parameter are not guaranteed.

2.22 Logic diagram

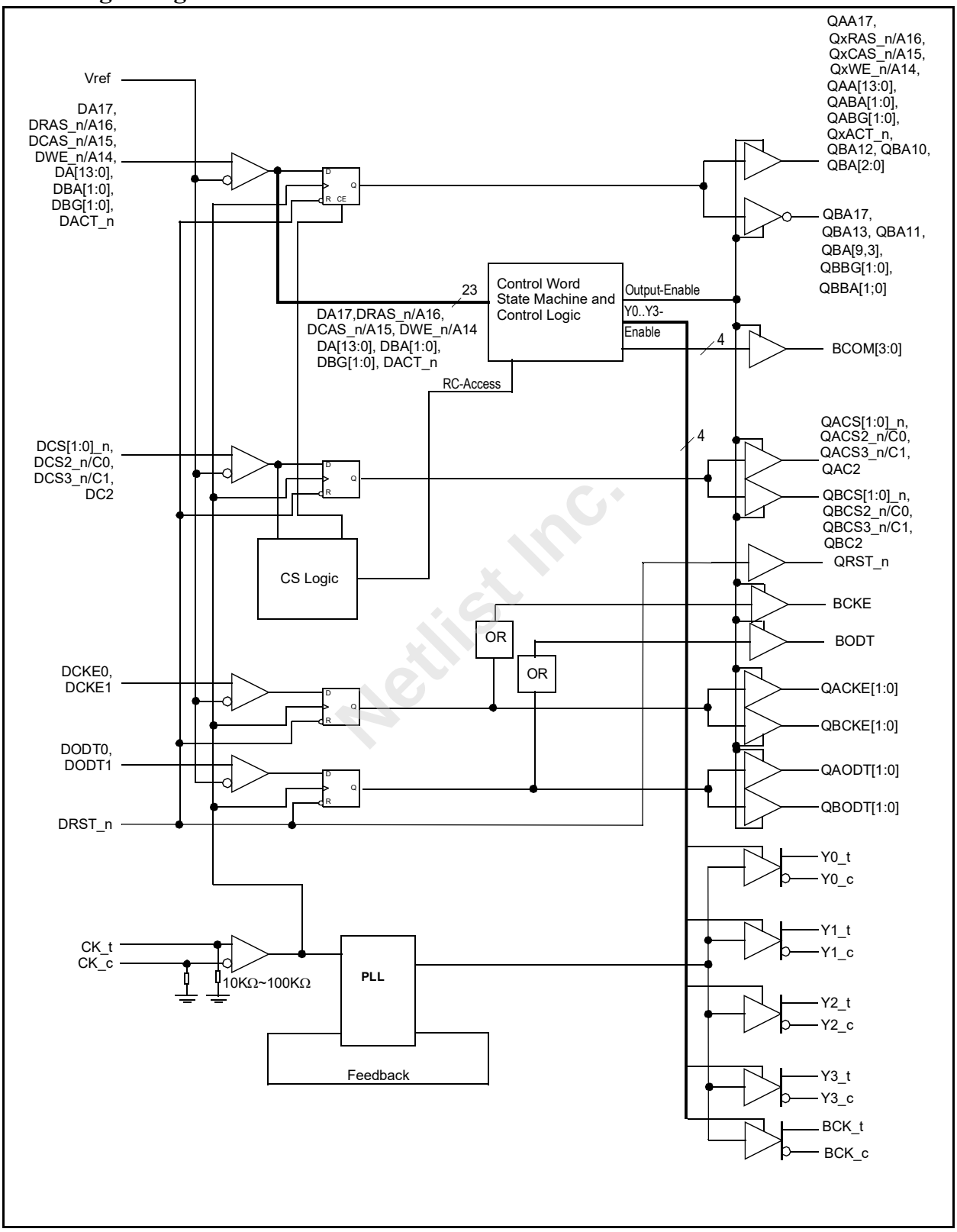


Figure 28 — Logic diagram (positive logic)

2.23 Control Words

The device features a set of control words, which allow the optimization of the device properties for different raw card designs. DDR4RCD02 control word (RCW) writes appear like DRAM MRS commands to MR7 which are ignored by the DDR4 DRAM. Each RCW write generates an MRS command to the rank 0 DRAMs behind the register, unless there is a parity error when parity checking is enabled, in which case both the RCW write as well as the MRS command to the DRAM are blocked. The different control words and settings are described below. Any change to these control words require some time for the device to settle. For changes to the control word setting, except for F0RC02 (DA3) and F0RC0A/F0RC3x, the controller needs to wait t_{MRD} after the last control word access, before further access to the DRAM can take place. For any changes to the clock timing (F0RC02: bit DA3, and F0RC0A/F0RC3x) this settling may take up to tSTAB time. All chip select inputs, DCS[n:0]_n, must be kept HIGH during that time.

The DDR4RCD02 contains 16 function spaces 0-15. Function spaces 0-7 are JEDEC defined or reserved for future use and Function spaces 8-15 are vendor specific. Function space 0 and 1 allocates decoding for up to 16 4-bit words of control bits (F[1:0]RC00 through F[1:0]RC0F) and up to 15 8-bit words of control bits. Only Function 0 can be accessed directly on the memory channel, reads or writes to Function spaces [15:1] can only be accessed through Function 0, by the combination of F0RC4x, F0RC5x and F0RC6x writes. Selection of each 4-bit control word is presented on inputs DA4 through DA12. Data to be written into the 4-bit configuration registers need to be presented on DA0 .. DA3. Selection of each 8-bit control word is presented on inputs DA8 through DA12. Data to be written into the 8-bit configuration registers need to be presented on DA0 .. DA7. Bits DA[16:14] must be LOW and at least one DCKEn input must be HIGH for a valid access. If register CKE power down feature is disabled, DCKEn inputs are don't care (either HIGH or LOW) during control word write operations, and are forwarded to the QxCKEn outputs. The DODT[1:0] inputs are also don't care (can be either HIGH or LOW), and are forwarded to the QxODT[1:0] outputs. Address and command parity is checked during control word write operations unless parity is disabled in the Parity Control Word. ALERT_n is asserted and the command is ignored if a parity error is detected.

Control word access must be possible in any valid frequency range in either of the two possible frequency bands.

2.23.1 Address Mirroring

Address mirroring allows for easier raw card routing by allowing specific pairs of address bits to be flipped on the back side of the board. The DDR4RCD02 allows address mirroring to be enabled on odd numbered ranks.

It is the host controller's responsibility to switch the address bits in an MRS command to accommodate address mirroring. This functionality is identical as to what is required for UDIMMs utilizing address mirroring.

The following is the address map for address mirroring.

Table 26 — Address Mirroring

Host bit (MB input)	Register output	Even rank DRAM connection	Odd rank DRAM connection, Mirroring off.	Odd Rank DRAM connection, Mirroring on	
DA0	QxA0	A0	A0	A0	A0 not swapped as it affects the burst start
DA1	QxA1	A1	A1	A1	A1 not swapped as it affects the burst start
DA2	QxA2	A2	A2	A2	A2 not swapped as it affects the burst start
DA3	QxA3	A3	A3	**A4**	A3 and A4 swapped
DA4	QxA4	A4	A4	**A3**	
DA5	QxA5	A5	A5	**A6**	A5 and A6 swapped
DA6	QxA6	A6	A6	**A5**	
DA7	QxA7	A7	A7	**A8**	A7 and A8 swapped
DA8	QxA8	A8	A8	**A7**	
DA9	QxA9	A9	A9	A9	
DA10	QxA10	A10	A10	A10	A10 cannot be swapped as it is Auto Precharge
DA11	QxA11	A11	A11	**A13**	A11 and A13 swapped
DA12	QxA12	A12	A12	A12	A12 cannot be swapped as it is Burst Length
DA13	QxA13	A13	A13	**A11**	A11 and A13 swapped
DA14	QxA14	A14	A14	A14	A14 cannot be swapped as it is WE_n
DA15	QxA15	A15	A15	A15	A15 cannot be swapped as it is CAS_n
DA16	QxA16	A16	A16	A16	A16 cannot be swapped as it is RAS_n
DA17	QxA17	A17	A17	A17	
DBA0	QxBA0	BA0	BA0	**BA1**	BA0 and BA1 swapped
DBA1	QxBA1	BA1	BA1	**BA0**	
DBG0	QxBG0	BG0	BG0	**BG1**	BG0 and BG1 swapped
DBG1	QxBG1	BG1	BG1	**BG0**	

Address signals can only be swapped if they perform no other special function. A0-2 set the burst start location for reads and writes, and cannot be swapped. A10 is the auto precharge bit for reads and writes. A12 is the burst length when burst on the fly is used for reads and writes. Address signals can only be swapped in pairs as shown in the above table.

During MRS cycles, the address bits contain register information, so all address bits must be in their proper location. This is done by having the host controller flip the bits when sending an MRS command to the DRAMs. Since MRS cycles are not a critical path, it does not affect performance by requiring the controller (or the BIOS) to do this muxing.

The DDR4RCD02 will always pass the address straight through during MRS commands. The DDR4RCD02 must know when mirroring is being used, however, as it snoops some specific address bits in order to use this information as part of its configuration, e.g. for sending A-side/B-side MRS commands to the DRAMs (see Chapter 2.9, “Output Inversion Enabling/Disabling,”).

2.23.2 Control Word Decoding

The control words are programmed by the host controller using the Rank 0 DRAM MRS function with DBG1, DBG0, DBA1, DBA0 = 0111. The DDR4RCD02 forwards the MRS command to the DRAM. The DRAM is required to ignore the content of this word.

The control word is clocked in when DCS0_n is LOW, DACT_n is HIGH and DA16/RAS_n, DA15/CAS_n, DA14/WE_n are LOW. In Encoded QuadCS mode, DC0 also has to be LOW for a valid control word access. Both the address of the control word and the settings are transmitted over DA[12:0].

The reset default state of all control words (except vendor specific ones) is '0'. Every time the device is reset, its default state is restored. Stopping the clocks (CK_t=CK_c=LOW) to put the device in low-power mode will not alter the control word settings.

Table 27 — Function Space 0 Control Word Decoding

Control word	Address Bit													Meaning
	12[1]	11	10	9	8	7	6	5	4	3	2	1	0	
F0RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				Global Features Control Word
F0RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				Clock Driver Enable Control Word
F0RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				Timing and IBT Control Word
F0RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				CA and CS Signals Driver Characteristics Control Word
F0RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				ODT and CKE Signals Driver Characteristics Control Word
F0RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Clock Driver Characteristics Control Word
F0RC06	0	0	0	0	0	0	1	1	0	command3:0]				Command Space Control Word
F0RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				LCOM[2:0] Interface Command Space Control Word
F0RC08	0	0	0	0	0	1	0	0	0	setting[3:0]				Input/Output Configuration Control Word
F0RC09	0	0	0	0	0	1	0	0	1	setting[3:0]				Power Saving Settings Control Word
F0RC0A	0	0	0	0	0	1	0	1	0	setting[3:0]				RDIMM Operating Speed
F0RC0B	0	0	0	0	0	1	0	1	1	setting[3:0]				Operating Voltage V_{DD} and VREF Source Control Word
F0RC0C	0	0	0	0	0	1	1	0	0	setting[3:0]				Training Control Word
F0RC0D	0	0	0	0	0	1	1	0	1	setting[3:0]				DIMM Configuration Control Word
F0RC0E	0	0	0	0	0	1	1	1	0	setting[3:0]				Parity Control Word
F0RC0F	0	0	0	0	0	1	1	1	1	setting[3:0]				Command Latency Adder Control Word
F0RC1x	0	0	0	0	1	setting[7:0]								Internal Vref Control Word
F0RC2x	0	0	0	1	0	setting[7:0]								I^2C Bus Control Word
F0RC3x	0	0	0	1	1	setting[7:0]								Fine Granularity RDIMM Operating Speed
F0RC4x	0	0	1	0	0	setting[7:0]								CW Source Selection Control Word
F0RC5x	0	0	1	0	1	setting[7:0]								CW Destination Selection Control Word
F0RC6x	0	0	1	1	0	setting[7:0]								CW Data Control Word
F0RC7x	0	0	1	1	1	setting[7:0]								IBT Control Word
F0RC8x	0	1	0	0	0	setting[7:0]								ODT Control Word
F0RC9x	0	1	0	0	1	setting[7:0]								QxODT[1:0] Write Pattern Control Word
F0RCAx	0	1	0	1	0	setting[7:0]								QxODT[1:0] Read Pattern Control Word
F0RCBx	0	1	0	1	1	setting[7:0]								IBT and MRS Snoop Control Word
F0RCCx .. F0RCFx	0	1	1	x	x	setting[7:0]								Error Log Register

1. Address bit 12 must be 0 for RCW accesses. Must be 1 for accesses to Data Buffer (DB) Control Words. If A12 = 1 for a CW write and the LRDIMM disable bit in F0RC0D is '0' (LRDIMM enabled), the RCD will generate a BCW Write command on the buffer control bus with the function space bits set to '000'. If a 'CW Write' command is executed via F0RC06 write and if A12 =1 in the CW Source Selection control word, the RCD02 will generate a BCW Write command on the buffer control bus with the function space bits from the CW Source Selection control word.

Table 28 — Function Space 1 Control Word Decoding[1]

Control word	Address Bit													Meaning
	12[1]	11	10	9	8	7	6	5	4	3	2	1	0	
F1RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				Data Buffer Interface Driver Characteristics Control Word
F1RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				CAL Mode Snoop enable
F1RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				CA and CS Output Slew Rate Control
F1RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				ODT and CKEn Output Slew Rate Control
F1RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				Clock Driver Output Slew Rate Control
F1RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Data Buffer Interface Output Slew Rate Control
F1RC06	0	0	0	0	0	0	1	1	0	setting[3:0]				Reserved for future use
F1RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved for future use
F1RC08	0	0	0	0	0	1	0	0	0	setting[3:0]				Reserved for future use
F1RC09	0	0	0	0	0	1	0	0	1	setting[3:0]				Reserved for future use
F1RC0A	0	0	0	0	0	1	0	1	0	setting[3:0]				Reserved for future use
F1RC0B	0	0	0	0	0	1	0	1	1	setting[3:0]				Reserved for future use
F1RC0C	0	0	0	0	0	1	1	0	0	setting[3:0]				Reserved for future use
F1RC0D	0	0	0	0	0	1	1	0	1	setting[3:0]				Reserved for future use
F1RC0E	0	0	0	0	0	1	1	1	0	setting[3:0]				Reserved for future use
F1RC0F	0	0	0	0	0	1	1	1	1	setting[3:0]				Reserved for future use
F1RC1x	0	0	0	0	1	setting[7:0]								QxCSn_n Output Delay Control
F1RC2x	0	0	0	1	0	setting[7:0]								QxCn Output Delay Control
F1RC3x	0	0	0	1	1	setting[7:0]								QxCKEn Output Delay Control
F1RC4x	0	0	1	0	0	setting[7:0]								QxODTn Output Delay Control
F1RC5x	0	0	1	0	1	setting[7:0]								QxCA Output Delay Control
F1RC6x	0	0	1	1	0	setting[7:0]								Y1/Y3 Output Delay Control
F1RC7x	0	0	1	1	1	setting[7:0]								Y0/Y2 Output Delay Control
F1RC8x	0	1	0	0	0	setting[7:0]								BCOM/BCKE/BODT Output Delay Control
F1RC9x	0	1	0	0	1	setting[7:0]								BCK Output Delay Control
F1RCAx	0	1	0	1	0	setting[7:0]								Reserved for future use
F1RCBx	0	1	0	1	1	setting[7:0]								Reserved for future use
F1RCCx	0	1	1	0	0	setting[7:0]								Reserved for future use
F1RCDx	0	1	1	0	1	setting[7:0]								Reserved for future use
F1RCEx	0	1	1	1	0	setting[7:0]								Reserved for future use
F1RCFx	0	1	1	1	1	setting[7:0]								Reserved for future use

1. Address bit 12 must be 0 for RCW accesses. Must be 1 for accesses to Data Buffer (DB) Control Words. If A12 = 1 for a CW write and the LRDIMM disable bit in F0RC0D is '0' (LRDIMM enabled), the RCD will generate a BCW Write command on the buffer control bus with the function space bits set to '000'. If a 'CW Write' command is executed via F0RC06 write and if A12 =1 in the CW Source Selection control word, the RCD02 will generate a BCW Write command on the buffer control bus with the function space bits from the CW Source Selection control word.

1. Function spaces [15:1] can only be accessed through Function 0 by the combinations of F0RC4x, F0RC5x and F0RC6x writes, however if the RCD supports the optional NVDIMM mode then Function space 4 can be accessed through F0RC07 but only on the LCOM[2:0] interface.

Function Space 4 contains Optional NVDIMM support feature Control Words. .

Table 29 — Function Space 4 Control Word Decoding[1]

Control word	Address Bit													Meaning
	12[1]	11	10	9	8	7	6	5	4	3	2	1	0	
F4RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				NVDIMM Mode Enable Control Word
F4RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				NVDIMM Asynchronous Interrupt Control Word
F4RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				Read Frame Gear Ratio and Yn/BCK Frequency Ratio Control Word
F4RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				LCOM Receiver Termination Control Word
F4RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				LCOM Receiver Vref Control Word
F4RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Reserved for future use
F4RC06	0	0	0	0	0	0	1	1	0	setting[3:0]				Reserved for future use
F4RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved for future use
F4RC08	0	0	0	0	0	1	0	0	0	setting[3:0]				Reserved for future use
F4RC09	0	0	0	0	0	1	0	0	1	setting[3:0]				Reserved for future use
F4RC0A	0	0	0	0	0	1	0	1	0	setting[3:0]				Reserved for future use
F4RC0B	0	0	0	0	0	1	0	1	1	setting[3:0]				Reserved for future use
F4RC0C	0	0	0	0	0	1	1	0	0	setting[3:0]				Reserved for future use
F4RC0D	0	0	0	0	0	1	1	0	1	setting[3:0]				Reserved for future use
F4RC0E	0	0	0	0	0	1	1	1	0	setting[3:0]				Reserved for future use
F4RC0F	0	0	0	0	0	1	1	1	1	setting[3:0]				Reserved for future use
F4RC1x	0	0	0	0	1	setting[7:0]								Multi Purpose Register
F4RC2x	0	0	0	1	0	setting[7:0]								Multi Purpose Register
F4RC3x	0	0	0	1	1	setting[7:0]								Multi Purpose Register
F4RC4x	0	0	1	0	0	setting[7:0]								Multi Purpose Register
F4RC5x	0	0	1	0	1	setting[7:0]								Data Transfer (Copy and Restore) Control Word
F4RC6x	0	0	1	1	0	setting[7:0]								Self-refresh Status Word
F4RC7x	0	0	1	1	1	setting[7:0]								Reserved for future use
F4RC8x	0	1	0	0	0	setting[7:0]								Reserved for future use
F4RC9x	0	1	0	0	1	setting[7:0]								Reserved for future use
F4RCAx	0	1	0	1	0	setting[7:0]								Reserved for future use
F4RCBx	0	1	0	1	1	setting[7:0]								Reserved for future use
F4RCCx	0	1	1	0	0	setting[7:0]								Reserved for future use
F4RCDx	0	1	1	0	1	setting[7:0]								Reserved for future use
F4RCEx	0	1	1	1	0	setting[7:0]								Reserved for future use
F4RCFx	0	1	1	1	1	setting[7:0]								Reserved for future use

1. Address bit 12 must be 0 for RCW accesses. Must be 1 for accesses to Data Buffer (DB) Control Words. If A12 = 1 for a CW write and the LRDIMM disable bit in F0RC0D is '0' (LRDIMM enabled), the RCD will generate a BCW Write command on the buffer control bus with the function space bits set to '000'. If a 'CW Write' command is executed via F0RC06 write and if A12 =1 in the CW Source Selection control word, the RCD02 will generate a BCW Write command on the buffer control bus with the function space bits from the CW Source Selection control word.

1. Function spaces [15-1] can only be accessed through Function 0 by the combination of F0RC4x, F0RC5x and F0RC6x writes, however if the RCD supports the optional NVDIMM mode then Function space 4 can be accessed through F0RC07 but only on the LCOM[2:0] interface.

Function Space 7 contains detailed RCD manufacturing information provided by RCD vendor. This information is programmed in OTP. The purpose is for improved manufacturing logistics management and not meant to be used by host platform to control normal operation. These registers must be accessible during run time.

Table 30 — Function Space 7 Control Word Decoding[1]

Control word	Address Bit													Meaning
	12[1]	11	10	9	8	7	6	5	4	3	2	1	0	
F7RC00	0	0	0	0	0	0	0	0	0	setting[3:0]				Reserved for future use
F7RC01	0	0	0	0	0	0	0	0	1	setting[3:0]				Reserved for future use
F7RC02	0	0	0	0	0	0	0	1	0	setting[3:0]				Reserved for future use
F7RC03	0	0	0	0	0	0	0	1	1	setting[3:0]				Reserved for future use
F7RC04	0	0	0	0	0	0	1	0	0	setting[3:0]				Reserved for future use
F7RC05	0	0	0	0	0	0	1	0	1	setting[3:0]				Reserved for future use
F7RC06	0	0	0	0	0	0	1	1	0	setting[3:0]				Reserved for future use
F7RC07	0	0	0	0	0	0	1	1	1	setting[3:0]				Reserved for future use
F7RC08	0	0	0	0	0	1	0	0	0	setting[3:0]				Reserved for future use
F7RC09	0	0	0	0	0	1	0	0	1	setting[3:0]				Reserved for future use
F7RC0A	0	0	0	0	0	1	0	1	0	setting[3:0]				Reserved for future use
F7RC0B	0	0	0	0	0	1	0	1	1	setting[3:0]				Reserved for future use
F7RC0C	0	0	0	0	0	1	1	0	0	setting[3:0]				Reserved for future use
F7RC0D	0	0	0	0	0	1	1	0	1	setting[3:0]				Reserved for future use
F7RC0E	0	0	0	0	0	1	1	1	0	setting[3:0]				Reserved for future use
F7RC0F	0	0	0	0	0	1	1	1	1	setting[3:0]				Reserved for future use
F7RC1x	0	0	0	0	1	setting[7:0]								Date code Byte 0[2] Year Information
F7RC2x	0	0	0	1	0	setting[7:0]								Date code Byte 1[2] Work Week Information
F7RC3x	0	0	0	1	1	setting[7:0]								Date code Byte 2[2] Reserved[2]
F7RC4x	0	0	1	0	0	setting[7:0]								Vendor specific unique unit code Byte 0[2]
F7RC5x	0	0	1	0	1	setting[7:0]								Vendor specific unique unit code Byte 1[2]
F7RC6x	0	0	1	1	0	setting[7:0]								Vendor specific unique unit code Byte 2[2]
F7RC7x	0	0	1	1	1	setting[7:0]								Vendor specific unique unit code Byte 3[2]
F7RC8x	0	1	0	0	0	setting[7:0]								Vendor specific unique unit code Byte 4[2]
F7RC9x	0	1	0	0	1	setting[7:0]								Vendor specific unique unit code Byte 5[2]
F7RCAx	0	1	0	1	0	setting[7:0]								Vendor specific unique unit code Byte 6[2]
F7RCBx	0	1	0	1	1	setting[7:0]								Vendor ID [7:0][3]
F7RCCx	0	1	1	0	0	setting[7:0]								Vendor ID [15:8][3]
F7RCDx	0	1	1	0	1	setting[7:0]								Device ID [7:0][3]
F7RCEx	0	1	1	1	0	setting[7:0]								Device ID [15:8][3]
F7RCFx	0	1	1	1	1	setting[7:0]								Revision ID [7:0][3]

1. Address bit 12 must be 0 for RCW accesses. Must be 1 for accesses to Data Buffer (DB) Control Words. If A12 = 1 for a CW write and the LRDIMM disable bit in F0RC0D is '0' (LRDIMM enabled), the RCD will generate a BCW Write command on the buffer control bus with the function space bits set to '000'. If a 'CW Write' command is executed via F0RC06 write and if A12 =1 in the CW Source Selection control word, the RCD02 will generate a BCW Write command on the buffer control bus with the function space bits from the CW Source Selection control word.
2. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.

1. Function spaces [15-1] can only be accessed through Function 0 by the combination of F0RC4x, F0RC5x and F0RC6x writes, however if the RCD supports the optional NVDIMM mode then Function space 4 can be accessed through F0RC07 but only on the LCOM[2:0] interface.

2.23.3 F0RC00 - Global Features Control Word

Table 31 — F0RC00: Global Features Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Output Inversion Disable[1]	Inversion Enabled
x	x	x	1		Inversion Disabled
x	x	0	x	Weak Drive[2]	Weak drive disabled
x	x	1	x		Weak drive enabled[3, 4]
x	0	x	x	A outputs disabled[5]	A outputs enabled
x	1	x	x		A outputs disabled
0	x	x	x	B outputs disabled[5]	B outputs enabled
1	x	x	x		B outputs disabled

1. For normal operation, output inversion is always enabled. For DIMM vendor test purpose, output inversion can be disabled. When disabled, register tPDM is not guaranteed to be met.
2. QxC[1:0] cannot have weak drive since the RCD could be on a DIMM that uses these outputs as chip selects.
3. When not actively driven the following drive strength of the following outputs is reduced: QxA0..QxA17, Qx-BA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR
4. See Table 126 for Weak Drive Impedance
5. For applications with reduced DRAM count, like Mini-RDIMM, the unused output side can be disabled to save power. All outputs are in Hi-Z in this case.

2.23.4 F0RC01 - Clock Driver Enable Control Word

Table 32 — F0RC01: Clock Driver Enable Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Disable Y0_t/Y0_c clock[1]	Y0_t/Y0_c clock enabled
x	x	x	1		Y0_t/Y0_c clock disabled
x	x	0	x	Disable Y1_t/Y1_c clock[1]	Y1_t/Y1_c clock enabled
x	x	1	x		Y1_t/Y1_c clock disabled
x	0	x	x	Disable Y2_t/Y2_c clock[1]	Y2_t/Y2_c clock enabled
x	1	x	x		Y2_t/Y2_c clock disabled
0	x	x	x	Disable Y3_t/Y3_c clock[1]	Y3_t/Y3_c clock enabled
1	x	x	x		Y3_t/Y3_c clock disabled

1. Output clocks may be individually turned on or off to conserve power. The system must read the module SPD to determine which clock outputs are used by the module. The PLL remains locked on CK_t/CK_c unless the system stops the clock inputs to the DDR4RCD02 to enter the lowest power mode.

2.23.5 F0RC02 - Timing and IBT Control Word

Table 33 — F0RC02: Timing and IBT Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	DA17 Input Bus Termination Disable[1]	Enabled
x	x	x	1		Disabled
x	x	0	x	DPAR Input Bus Termination Disable[1]	Enabled
x	x	1	x		Disabled
x	0	x	x	Transparent Mode	Disabled
x	1	x	x		Enabled
0	x	x	x	Frequency Band Select	Operation (Frequency Band 1)
1	x	x	x		Test Mode (Frequency Band 2)

1. F0RC02, DA[1:0] = 11 has priority over any value specified in RC7x for DA17 and DPAR.

2.23.6 F0RC03 - CA and CS Signals Driver Characteristics Control Word

Table 34 — F0RC03: CA and CS Signals Driver Characteristics Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	Address/Command - QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR, QxC0[1] QxC1[1]	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Strong Drive (16 or 20 DRAM Loads)
x	x	1	1		Very Strong Drive (32 or 40 Loads)
0	0	x	x	QxCS0_n ,QxCS1_n, QxCS2_n[1]QxCS3_n [1]Outputs	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Strong Drive (16 or 20 DRAM Loads)
1	1	x	x		Very Strong Drive (32 or 40 Loads)

1. If QxC0/QxCS2_n and QxC1/QxCS3 are configured as QxC0 and QxC1 then drive strengths are defined by F0RC03 DA[1:0]. If QxC0/QxCS2_n and QxC1/QxCS3_n are configured as QxC2S_n and QxCS3_n then drive strengths are defined by F0RC03 DA[3:2]

2.23.7 F0RC04 - ODT and CKE Signals Driver Characteristics Control Word

Table 35 — F0RC04: ODT and CKE Signals Driver Characteristics Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	QxODT0 .. QxODT1 Outputs	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Strong Drive (16 or 20 DRAM Loads)
x	x	1	1		Very Strong Drive (32 or 40 Loads)
0	0	x	x	QxCKE0 .. QxCKE1 Outputs	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Strong Drive (16 or 20 DRAM Loads)
1	1	x	x		Very Strong Drive (32 or 40 Loads)

2.23.8 F0RC05 - Clock Driver Characteristics Control Word

Table 36 — F0RC05: Clock Driver Characteristics Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	Clock Y1_t, Y1_c, Y3_t, and Y3_c Output Drivers (A side)	Light Drive (4 or 5 DRAM Loads)
x	x	0	1		Moderate Drive (8 or 10 DRAM Loads)
x	x	1	0		Strong Drive (16 or 20 DRAM Loads)
x	x	1	1		Very Strong Drive (32 or 40 Loads)
0	0	x	x	Clock Y0_t, Y0_c, Y2_t, and Y2_c Output Drivers (B side)	Light Drive (4 or 5 DRAM Loads)
0	1	x	x		Moderate Drive (8 or 10 DRAM Loads)
1	0	x	x		Strong Drive (16 or 20 DRAM Loads)
1	1	x	x		Very Strong Drive (32 or 40 Loads)

2.23.9 F0RC06 - Command Space Control Word

After issuing a register command via writes to F0RC06 waiting for t_{MRC} is required before the next DRAM command or CW write can be issued. .

Table 37 — F0RC06: Command Space Control Word definition

Cmd (DA[3:0])				Command No	Command Name	Result
0	0	0	0	CMD 0	SoftReset[1]	Resets state of RCD. Sends reset to DB for 16 * tCK. Self Clear in the next cycle. Does NOT cause QRST_n assertion.
0	0	0	1	CMD 1	DB Reset	Sends reset to DB for 16 * tCK. Does NOT reset RCD.
0	0	1	0	CMD 2	DRAM Reset	Switches QRST_n to active which is low
0	0	1	1	CMD 3	Clear DRAM Reset	Switches QRST_n to inactive which is high
0	1	0	0	CMD 4	CW Read Operation[2]	Sends selected CW (in CW source selection control word) to DRAM MPR page 0 of the rank 0 DRAMs
0	1	0	1	CMD 5	CW Write Operation	Writes "data" in CW data control word to selected CW (in CW source selection control word)
0	1	1	0	CMD 6	Clear CA Parity Error	Clear 'CA Parity Error Status' bit and '> 1 Error' bit and re-enable parity checking (if not already enabled)
0	1	1	1	CMD 7	Gear-down Mode Delay CS	Delay chip select for next command by 1 nCK
1	0	0	0	CMD 8	Gear-down Mode Entry	RCD enters CTRL Gear-down Mode
1	0	0	1	CMD 9	Soft RCD Reset[1,3,4]	Resets state of RCD. Self Clear in the next cycle. Does NOT cause QRST_n assertion and does NOT send reset to DB.
1	0	1	0	CMD 10	Gear-down Mode Exit	RCD exits CTRL Gear-down Mode or Delay CS Mode and returns to 1N
1	0	1	1	CMD 11	Reserved	Reserved
1	1	0	0	CMD 12	Reserved	Reserved
1	1	0	1	CMD 13	Reserved	Reserved
1	1	1	0	CMD 14	Reserved	Reserved
1	1	1	1	CMD 15	NOP	No Operation[5]

1. Requires waiting for t_{STAB}
2. The RCD is responsible for sending an MPR Write command to the DRAMs with QABA[1:0]=F0RC5x[6:5] and QAA[7:0] = F0RC6X[7:0].The host controller is responsible for sending MRS to MR3 to enable MPR mode in the DRAMs prior to issuing 'CW Read Operation'. The host is also responsible for issuing the MPR Read command to the DRAMs after issuing 'CW Read Operation'.
3. The DDR4DB02 or DRAM must not be PDA mode, the DDR4DB02 must not be in MPR Read override mode or BCW Read mode and the DDR4DB02 F[7:0]BC7x control word should cleared before issuing a Soft RCD Reset.
4. For LRDIMM during Soft RCD Reset the DDR4DB02 must be in CKE Power Down Mode.
5. This operation was added specifically for hosts that don't support byte writes over the I^2C Bus, i.e. that have to write more than one RCW at the same time.

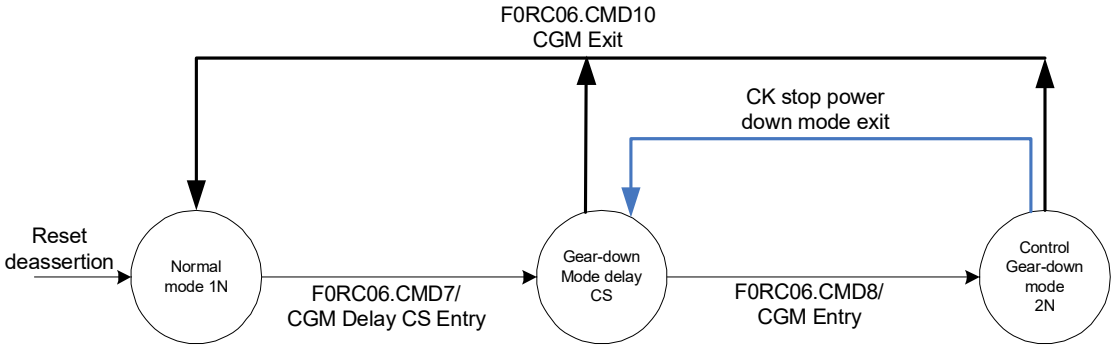


Figure 29 — Gear-down and Delay CS Mode Exit

NOTE 1 When in Control Gear-down Mode a CK stop power down event will return RCD to Delay CS Mode

NOTE 2 CMD 10 will return RCD to 1N mode from either Gear-down Delay CS Mode or Gear-down Mode.

2.23.10 F0RC07 - LCOM[2:0] Interface Command Space Control Word

If the optional NVDIMM mode feature is supported, control word F0RC07 must be implemented. When F4RC00 - DA0 is set to 1 (NVDIMM mode enabled) the F0RC07 control word can only be written through the LCOM[2:0] interface regardless of the settings programmed in F4RC00 - DA[2:1]. When F4RC00 - DA0 = 1, F0RC07 cannot be accessed for reads or writes through the Host CTRL/CMD/ADD or I^2C interfaces (i.e., it will be treated as a reserved location).

Table 38 — F0RC07: LCOM[2:0] Interface Command Space Control Word definition

Cmd (DA[3:0])				Command No	Command Name	Result
0	0	0	0	CMD 0	NOP	No Operation[1]
0	0	0	1	CMD 1	Reserved	Reserved
0	0	1	0	CMD 2	Reserved	Reserved
0	0	1	1	CMD 3	Reserved	Reserved
0	1	0	0	CMD 4	RCW Read through LCOM	Sends control words F4RC1x .. F4RC4x (designated CW if F4RC00 - DA[1:0] = '01') or selected CW (in CW source selection control word) to RCD02 LCOM bus[2]
0	1	0	1	CMD 5	Use Function Space 4 in RCW Write	Use Function Space 4 for the next RCW Write command (Rank 0, A-side MRS to MR7)[3]
0	1	1	0	CMD 6	Reserved	Reserved
0	1	1	1	CMD 7	Reserved	Reserved
1	0	0	0	CMD 8	Reserved	Reserved
1	0	0	1	CMD 9	Reserved	Reserved
1	0	1	0	CMD 10	Reserved	Reserved
1	0	1	1	CMD 11	Reserved	Reserved
1	1	0	0	CMD 12	Reserved	Reserved
1	1	0	1	CMD 13	Reserved	Reserved
1	1	1	0	CMD 14	Reserved	Reserved
1	1	1	1	CMD 15	Reserved	Reserved

1. This operation was added for backward compatibility with Hosts that don't support byte writes over the I^2C Bus, i.e. that have to write more than one RCW at the same time and which have been designed to program all bits of empty control word locations with zeros.
2. This command sets up the LCOM[2:0] interface to start an RCW data transfer in response to the next start HIGH pulse on signal LCOM2 as illustrated in Table 18, "LCOM[2:0] Read Data Frame Definition (Gear Ratio = 2 Selected in F4RC02 - DA[1:0])". This command does not result in any transfer of information or commands to the DRAMs, since it is intended for NVDIMM support through the LCOM[2:0] interface.
3. RCD02 logic returns to normal operation after a single Rank 0, A-side MRS to MR7 command is received.

2.23.11 F0RC08 - Input/Output Configuration Control Word

Table 39 — F0RC08: Input/Output Configuration Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	QxC[2:0] outputs disabled[1,2,3,4]	QxC[2:0] enabled
x	x	0	1		QxC[1:0] enabled, QxC2 disabled
x	x	1	0		QxC[2:1]disabled, QxC0 enabled[5]
x	x	1	1		QxC[2:0] disabled
x	0	x	x	QxPAR outputs disabled[6,7]	Outputs enabled
x	1	x	x		Outputs disabled
0	x	x	x	DA17 Input Buffer and QxA17 outputs disabled[4]	Enabled
1	x	x	x		Disabled

1. QAC[2:0] and QBC[2:0] outputs are only enabled if the corresponding output group is also enabled in F0RC00.
2. These control bits are in effect regardless of whether QxC[1:0] are used as chip IDs or as chip selects.
3. QxC[1:0] must be enabled if they are used as chip selects in one of the QuadCS modes. Chip selects are never included in the parity calculation.

4. Refer to Table 40 for the conditions that determine if this signal is included in parity calculation. The register disables the corresponding input receivers if these outputs are disabled. Refer to Table 61 for the IBT enable/ disable settings for the corresponding inputs.
5. DC0 is not included in the parity calculation in Encoded QuadCS mode.
6. QBPAR will be inverted relative to DPAR if F0RC08 DA3 = 1.
7. If the QxPAR outputs are disabled (F0RC08 DA2 = 1) and parity checking is disabled (F0RC0E DA0 = 0) the DPAR input receiver will be disabled.

Table 40 — Parity Checking and DC[2:0] & DA17 Inputs

Mode	F0RC0D DA[1:0] Setting	Conditions to Include Signal in Parity Calculation			
		DC0	DC1	DC2	DA17
Direct DualCS	00	F0RC08 DA[1:0] = 00, 01, 10	F0RC08 DA[1:0] = 00, 01	F0RC08 DA[1:0] = 00	F0RC08 DA3 = 0
Direct QuadCS	01	Never	Never	F0RC08 DA[1:0] = 00	F0RC08 DA3 = 0
Encoded QuadCS	11	Never	Never	F0RC08 DA[1:0] = 00	F0RC08 DA3 = 0

2.23.12 F0RC09 - Power Saving Settings Control Word

Table 41 — F0RC09: Power Saving Settings Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	DCS1 Input Bus Termination Disable[1]	Enabled
x	x	x	1		Disabled
x	x	0	x	DCS1 Input Buffer & QxCS1 Outputs Disable[2]	Enabled
x	x	1	x		Disabled
1	0	x	x	CKE Power Down Mode[3]	CKE power down with IBT ON: QxODT are a function of DODTx if F0RC8x DA[7:6] is configured as '00' or '01'. If F0RC8x DA[7:5] is configured as either '000' or '010', then BODT is a function of DODTn.
1	1	x	x		CKE power down with IBT OFF, QxODT held LOW. If the BODT output is enabled, it is held LOW.
0	x	x	x	CKE Power Down Mode Enable[4]	Disabled
1	x	x	x		Enabled

1. F0RC09, DA0 = 1 has priority over any value specified in F0RC7x for DCS1.
2. The host must program F0RC0D DA[1:0] to '00' or '11' when F0RC09 DA1 is set to '1'.
3. The register ignores CKE Power Down mode setting when CKE Power Down is disabled by F0RC09 DA3.
4. CKE power down is invoked once both DCKE0 and DCKE1 are LOW.

2.23.13 F0RC0A - DIMM Operating Speed

Table 42 — F0RC0A: DIMM Operating Speed[1]

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	f ≤ 1600 MT/s	DDR4-1600
x	0	0	1	1600 MT/s < f ≤ 1866 MT/s	DDR4-1866
x	0	1	0	1866 MT/s < f ≤ 2133 MT/s	DDR4-2133
x	0	1	1	2133 MT/s < f ≤ 2400 MT/s	DDR4-2400
x	1	0	0	2400 MT/s < f ≤ 2666 MT/s	DDR4-2666
x	1	0	1	2666 MT/s < f ≤ 2933 MT/s	DDR4-2933
x	1	1	0	2933 MT/s < f ≤ 3200 MT/s	DDR4-3200
x	1	1	1	PLL Bypass Mode	PLL bypass mode enabled
0	x	x	x	Context for operation training	Default; Context 1 operation
1	x	x	x		Context 2 operation[2]

1. The encoding value is used to inform the register the operating speed that it is being run at in a system. It is not an indicator of how fast or slow a register can run.

2. F0RC03, F0RC04, F0RC05, F0RC0F, F0RC1x, F0RC5x DA[3:0], F0RC7x, F0RC8x DA[4:0], F0RC9x, F0RCAx, F1RC00, F1RC1x, F1RC2x, F1RC3x, F1RC4x, F1RC5x, F1RC6x, F1RC7x, F1RC8x, and F1RC9x are duplicated by the RCD02 for the 2nd frequency context.

2.23.14 F0RC0B - Operating Voltage V_{DD} and VrefCA Source Control Word

Table 43 — F0RC0B: Operating Voltage V_{DD} and VrefCA Source Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Register V_{DD} Operating Voltage[1]	1.2 V
x	x	x	1		Reserved for lower voltage
x	0	0	x	QVrefCA and BVrefCA Sources	$V_{DD}/2$[2] connected to QVrefCA and BVrefCA
x	0	1	x		Internally generated Vref connected to QVrefCA[3] $V_{DD}/2$[2] connected to BVrefCA
x	1	0	x		Internally generated Vref connected to BVrefCA[3] $V_{DD}/2$[2] connected to QVrefCA
x	1	1	x		External VrefCA input connected to QVrefCA and BVrefCA
0	x	x	x	Input Receiver Vref Source	Internally generated Vref[3]
1	x	x	x		External VrefCA input

1. F0RC0B will be used to inform DDR4RCD02 under what operating voltage V_{DD} will be used. Register can use the information to optimize their functionality and performance at low voltage conditions.
2. $V_{DD}/2$ is also internally generated, but not by the VrefCA DAC.
3. Value programmed in F0RC1x. There is only one internal Vref generator. If more than one destination is configured for internally generated Vref, then they will all receive the same Vref level.

2.23.15 F0RC0C - Training Control Word

Table 44 — F0RC0C: Training Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	Training mode selection	Normal operating mode
x	0	0	1		Clock-to-CA training mode[1]
x	0	1	0		DCS0_n loopback mode[1]
x	0	1	1		DCS1_n loopback mode[1]
x	1	0	0		DCKE0 loopback mode[1]
x	1	0	1		DCKE1 loopback mode[1]
x	1	1	0		DODT0 loopback mode[1]
x	1	1	1		DODT1 loopback mode[1]
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

1. In these training modes the DDR4RCD02 samples the affected inputs every other clock cycle (to accommodate the host sending alternating '0' and '1' pattern on these signals).

2.23.16 F0RC0D - DIMM Configuration Control Word

Table 45 — F0RC0D: DIMM Configuration Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	CS mode	Direct DualCS mode: Register uses two DCS_n inputs (DCS0_n and DCS1_n)
x	x	0	1		Direct QuadCS mode: Register uses four DCSx_n inputs. In this mode DC0 becomes DCS2_n and DC1 becomes DCS3_n.
x	x	1	0		Reserved
x	x	1	1		Encoded QuadCS mode: Register uses DC0 to decode four QxCSy_n outputs from two DCSx_n inputs
x	0	x	x	DIMM Type	LRDIMM[1]
x	1	x	x		RDIMM[2]
0	x	x	x	Address mirroring for MRS commands	Disabled
1	x	x	x		Enabled. Register is aware that address mirroring is used for odd ranks.

1. BODT, BCKE, BCOM, BCK_t/BCK_c and BVrefCA output drivers are enabled. BODT output driver is disabled if F0RC8x DA[7:6] is configured as '10' or if F0RC8x DA5 is set to '1'.
2. BODT, BCKE, BCOM, BCK_t/BCK_c and BVrefCA output drivers are disabled.

2.23.17 F0RC0E - Parity, NV Mode Enable, and ALERT Configuration Control Word

Table 46 — F0RC0E: Parity , NV Mode Enable, and ALERT Configuration Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	Parity Enable	Parity checking disabled[1]
x	x	x	1		Parity checking enabled. Command[2] must be delayed[3,4]
x	x	0	x	NV Mode Enable Lock[5]	(Default) NV Mode enable (F4RC00 - DA0) can be modified
x	x	1	x		NV Mode enable (F4RC00 - DA0) cannot be modified.[6]
x	0	x	x	ALERT_n Assertion[7]	ALERT_n stays asserted until 'Clear CA Parity Error' command is sent
x	1	x	x		ALERT_n pulse width according to Table 47
0	x	x	x	ALERT_n Re-enable[8]	Parity checking remains disabled after ALERT_n pulse
1	x	x	x		Parity checking is re-enabled after ALERT_n pulse

1. Register does not check for parity including control word programming.
2. Command includes QxA0 .. QxA17, QxBA0 .. QxBA1, QxBG0 .. QxBG1, QxACT_n, QxC0 .. QxC2, QxCKE0/1, QxODT0/1, QxCS0_n .. QxCS3. It also includes BCOM[3:0], BODT and BCKE if the buffer control bus is enabled. QxPAR is driven in the same cycle as the command (if outputs are enabled).
3. As specified in Table 48
4. At least 1 nCK for $\leq$ 2400MT/s; at least 2 nCK for > 2400MT/s
5. This optional control bit must be implemented if the NVDIMM mode feature is supported. This is a "Write 1 Only" register. It can only be set (i.e., write '1') but not reset (i.e., write '0') via I^2C or RCW Write command. Only hardware DRST_n pin clears NV Mode Enable Lock. This control bit is not cleared by F0RC06 CMD 0 'Soft Reset' or CMD 9 'Soft RCD Reset'.
6. When F0RC0E - DA1 is written to 1, the NV Mode Enable control bit F4RC00 - DA0 will no longer be writable and the RCD02 will remain in NV Mode Disabled state (if F4RC00 - DA0 = 0) or NV Mode Enabled state (if F4RC00 - DA0 = 1) until a DRST_n reset event is applied to the RCD02 device.
7. This bit only affects ALERT_n assertion that is a result of a CA parity error. In case of a LOW level on the ERROR_IN_n input, ALERT_n stays asserted as long as ERROR_IN_n remains LOW unless DRST_n is LOW or the device is in clock stopped power down mode.
8. CA Parity Error Status bit in Error Log Register remains set until cleared by sending a Clear CA Parity Error command.

Table 47 — ALERT_n Pulse Width

DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4 - 2666		DDR4 - 2933		DDR4 - 3200		Units
Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
48	96	56	112	64	128	72	144	80	160	88	176	96	192	nCK

Figure 25 shows DCSx assertion are not permitted t_{CSALT} prior and after of ALERT_n de-assertion when F0RC0E DA2 =1.

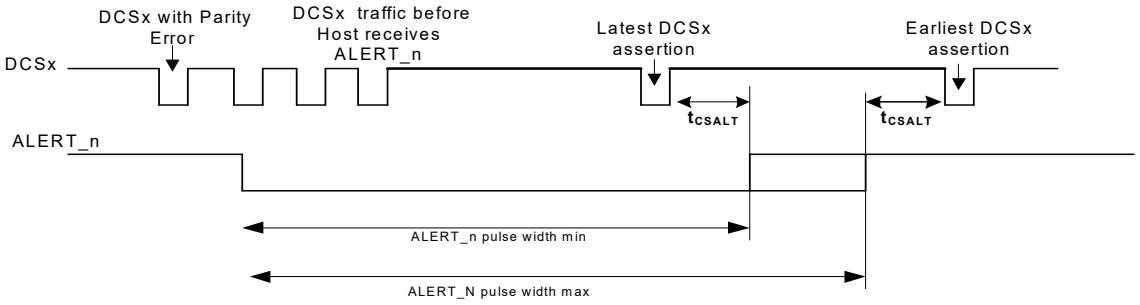


Figure 30 — DCSx Assertion during ALERT_n Pulse Width

2.23.18 F0RC0F - Command Latency Adder Control Word

When parity checking feature is enabled, at least 1 nCK Latency Adder is required. During Control Gear-down mode, the odd number of nLadd can't be supported since RCD will use a divided clock to sample the input signals

Table 48 — F0RC0F: Command Latency Adder Control Word

Setting (DA[3:0])				Definition	Encoding
x	0	0	0	Latency adder nLadd to all DRAM commands	1 nCK latency adder to Qn[1], QxCSn, QxCKEn[2], QxODTn 0nCK latency adder to QxPAR
x	0	0	1		2 nCK[3] latency adder to Qn[1], QxCSn, QxCKEn[2], QxODTn 1nCK latency adder to QxPAR[4](0 nCK latency adder to QxPAR if CTRL Gear-down mode is enabled)
x	0	1	0		3 nCK latency adder to Qn[1], QxCSn, QxCKEn[2], QxODTn 2nCK latency adder to QxPAR[4]
x	0	1	1		4 nCK[3] latency adder to Qn[1], QxCSn, QxCKEn[2], QxODTn 3nCK latency adder to QxPAR[4](2 nCK latency adder to QxPAR if CTRL Gear-down mode is enabled)
x	1	0	0		0 nCK latency adder[4,5]
x	1	0	1		Reserved
x	1	1	0		Reserved
x	1	1	1		Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

1. Qn = QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2
2. Only falling (i.e. HIGH to LOW) edges of DCKEn are delayed by nLadd. Rising (i.e. LOW to HIGH) edges of DCKEn are immediately forwarded to QxCKEn.
3. Only nLadd of 2 nCK and 4 nCK can be supported when Control Gear-down Mode is enabled.
4. The correct frequency range has to be programmed in F0RC0A before any changes to F0RC0F from the power-on default are allowed
5. 0 nCK setting is only valid if parity checking and CAL modes are disabled

2.23.19 F0RC1x - Internal VrefCA Control Word

Table 49 — F0RC1x: Internal VrefCA Control Word

Cmd (DA[7:0])								VrefCA as% of V_{DD}[1]	Comment
0	0	0	0	0	0	0	0	50.0%	$V_{DD}/2$
0	0	0	0	0	0	0	1	50.83%	$V_{DD}/2$ + 0.833%.
0	0	0	0	0	0	1	0	51.67%	$V_{DD}/2$ + 1.67%
0	0	0	0	0	0	1	1	52.60%	$V_{DD}/2$ + 2.60%
0	0	0	0	0	1	0	0	53.33%	$V_{DD}/2$ + 3.33%
0	0	0	0	0	1	0	1	54.17%	$V_{DD}/2$ + 4.17%
0	0	0	0	0	1	1	0	55.00%	$V_{DD}/2$ + 5.00%
0	0	0	0	0	1	1	1	55.83%	$V_{DD}/2$ + 5.83%
0	0	0	0	1	0	0	0	56.67%	$V_{DD}/2$ + 6.67%
0	0	0	0	1	0	0	1	57.50%	$V_{DD}/2$ + 7.50%
0	0	0	0	1	0	1	0	58.33%	$V_{DD}/2$ + 8.33%
0	0	0	0	1	0	1	1	59.17%	$V_{DD}/2$ + 9.17%
0	0	0	0	1	1	0	0	60.00%	$V_{DD}/2$ + 10.00%
0	0	0	0	1	1	0	1	60.83%	$V_{DD}/2$ + 10.83%
0	0	0	0	1	1	1	0	61.67%	$V_{DD}/2$ + 11.67%
0	0	0	0	1	1	1	1	62.50%	$V_{DD}/2$ + 12.50%
0	0	0	1	0	0	0	0	63.33%	$V_{DD}/2$ + 13.33%
0	0	0	1	0	0	0	1	64.17%	$V_{DD}/2$ + 14.17%
0	0	0	1	0	0	1	0	65.00%	$V_{DD}/2$ + 15.00%
0	0	0	1	0	0	1	1	65.83%	$V_{DD}/2$ + 15.83%
0	0	0	1	0	1	0	0	66.67%	$V_{DD}/2$ + 16.67%
0	0	0	1	0	1	0	1	Reserved	Reserved for future use
0	0	0	1	0	1	1	0	Reserved	Reserved for future use
0	0	0	1	0	1	1	1	Reserved	Reserved for future use
0	0	0	1	1	x	x	x	Reserved	Reserved for future use
0	0	1	0	0	x	x	x	Reserved	Reserved for future use
0	0	1	0	1	0	x	x	Reserved	Reserved for future use
0	0	1	0	1	1	0	0	33.33%	$V_{DD}/2$ - 16.67%
0	0	1	0	1	1	0	1	34.17%	$V_{DD}/2$ - 15.83%
0	0	1	0	1	1	1	0	35.00%	$V_{DD}/2$ - 15.00%
0	0	1	0	1	1	1	1	35.83%	$V_{DD}/2$ - 14.17%
0	0	1	1	0	0	0	0	36.67%	$V_{DD}/2$ - 13.33%
0	0	1	1	0	0	0	1	37.50%	$V_{DD}/2$ - 12.50%
0	0	1	1	0	0	1	0	38.33%	$V_{DD}/2$ - 11.67%
0	0	1	1	0	0	1	1	39.17%	$V_{DD}/2$ - 10.833%
0	0	1	1	0	1	0	0	40.00%	$V_{DD}/2$ - 10.00%
0	0	1	1	0	1	0	1	40.83%	$V_{DD}/2$ - 9.17%
0	0	1	1	0	1	1	0	41.67%	$V_{DD}/2$ - 8.33%
0	0	1	1	0	1	1	1	42.50%	$V_{DD}/2$ - 7.50%
0	0	1	1	1	0	0	0	43.33%	$V_{DD}/2$ - 6.67%
0	0	1	1	1	0	0	1	44.17%	$V_{DD}/2$ - 5.83%
0	0	1	1	1	0	1	0	45.00%	$V_{DD}/2$ - 5.00%
0	0	1	1	1	0	1	1	45.83%	$V_{DD}/2$ - 4.17%
0	0	1	1	1	1	0	0	46.67%	$V_{DD}/2$ - 3.33%
0	0	1	1	1	1	0	1	47.50%	$V_{DD}/2$ - 2.50%
0	0	1	1	1	1	1	0	48.33%	$V_{DD}/2$ - 1.67%
0	0	1	1	1	1	1	1	49.17%	$V_{DD}/2$ - 0.833%
0	1	x	x	x	x	x	x	Reserved	Reserved for future use
1	0	x	x	x	x	x	x	Reserved	Reserved for future use
1	1	x	x	x	x	x	x	Reserved	Reserved for future use

1. These are targetVrefCA values. Acceptable actual values are determined based on tolerances defined in electrical section.

2.23.20 I²C Bus Control Words

Table 50 — F0RC2x: I²C Bus Control Word and Function Space Context

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	I²C Bus Interface Disabled	I²C Bus interface is enabled
x	x	x	x	x	x	x	1		I²C Bus interface is disabled. DDR4RCD02 will not claim or acknowledge any access to its I²C Bus address space.
x	x	x	x	x	x	0	x	I²C Bus Read Access Control to function space 0	I²C Bus read accesses from FN0 return data
x	x	x	x	x	x	1	x		I²C Bus reads from FN0 return all ones[1]
x	x	x	x	x	0	x	x	I²C Bus Write Access Control to function space 0	I²C Bus write accesses to FN0 are executed
x	x	x	x	x	1	x	x		I²C Bus writes to FN0 are not acknowledged and not executed
x	x	x	x	0	x	x	x	I²C Bus Read Access Control to function spaces 1 to 7	I²C Bus read accesses from FN1-7 return data
x	x	x	x	1	x	x	x		I²C Bus reads from FN1-7 return all ones[1]
x	x	x	0	x	x	x	x	I²C Bus Write Access Control to function spaces 1 to 7	I²C Bus write accesses to FN1-7 are executed
x	x	x	1	x	x	x	x		I²C Bus writes to FN1-7 are not acknowledged and not executed
x	x	0	x	x	x	x	x	F0RC4x CW Source Selection Context for RCD	Context 1 (Function space 0 -7)
x	x	1	x	x	x	x	x		Context 2 (Function space 8-15)[2,3]
x	0	x	x	x	x	x	x	I²C Bus Read Access Control to function spaces 8 to 15	I²C Bus read accesses from FN8-15 return data
x	1	x	x	x	x	x	x		I²C Bus reads from FN8-15 return all ones[1]
0	x	x	x	x	x	x	x	I²C Bus Write Access Control to function spaces 8 to 15	I²C Bus write accesses to FN8-15 are executed
1	x	x	x	x	x	x	x		I²C Bus writes to FN8-15 are not acknowledged and not executed

1. DDR4RCD02 returns the status of "Internal Target Abort". The host controller should not try to access this through I²C Bus. However, if the host ignores this then DDR4RCD02 will return all ones.
2. CW Source Selection Context 2 bit DA5 is set to access vendor specific function spaces 8-15, it is the responsibility of the DDR4RCD02 to clear F0RC2x bit DA5 after accessing any of the function spaces 8-15.
3. F0RC2x DA5 only applies when accessing RCD function space and is not used when accessing Data Buffer function spaces.

2.23.21 F0RC3x - Fine Granularity RDIMM Operating Speed

Table 51 — F0RC3x: Fine Granularity RDIMM Operating Speed[1]

Setting (DA[7:0])								Definition	Encoding[2]
x	0	0	0	0	0	0	0	Fine Granularity Operating Speed[3,4,5]	1240 MT/s < f ≤ 1260 MT/s
x	0	0	0	0	0	0	1		1260 MT/s < f ≤ 1280 MT/s
x	0	0	0	0	0	1	0		1280 MT/s < f ≤ 1300 MT/s
x	0	0	0	0	0	1	1		1300 MT/s < f ≤ 1320 MT/s
x	0	0	0	0	1	0	0		1320 MT/s < f ≤ 1340 MT/s
x	0	0	0	0	1	0	1		1340 MT/s < f ≤ 1360 MT/s
x	0	0	0	0	1	1	0		1360 MT/s < f ≤ 1380 MT/s
x	0	0	0	0	1	1	1		1380 MT/s < f ≤ 1400 MT/s
x	0	0	0	1	0	0	0		1400 MT/s < f ≤ 1420 MT/s
x	0	0	0	1	0	0	1		1420 MT/s < f ≤ 1440 MT/s
x	0	0	0	1	0	1	0		1440 MT/s < f ≤ 1460 MT/s
x	0	0	0	1	0	1	1		1460 MT/s < f ≤ 1480 MT/s
x	0	0	0	1	1	0	0		1480 MT/s < f ≤ 1500 MT/s
x	0	0	0	1	1	0	1		1500 MT/s < f ≤ 1520 MT/s
x	0	0	0	1	1	1	0		1520 MT/s < f ≤ 1540 MT/s
x	0	0	0	1	1	1	1		1540 MT/s < f ≤ 1560 MT/s
x	0	0	1	0	0	0	0		1560 MT/s < f ≤ 1580 MT/s
x	0	0	1	0	0	0	1		1580 MT/s < f ≤ 1600 MT/s
x	0	0	1	0	0	1	0		1600 MT/s < f ≤ 1620 MT/s
x	0	0	1	0	0	1	1		1620 MT/s < f ≤ 1640 MT/s
x	0	0	1	0	1	0	0		1640 MT/s < f ≤ 1660 MT/s
x	0	0	1	0	1	0	1		1660 MT/s < f ≤ 1680 MT/s
x	0	0	1	0	1	1	0		1680 MT/s < f ≤ 1700 MT/s
x	0	0	1	0	1	1	1		1700 MT/s < f ≤ 1720 MT/s
x	0	0	1	1	0	0	0		1720 MT/s < f ≤ 1740 MT/s
x	0	0	1	1	0	0	1		1740 MT/s < f ≤ 1760 MT/s
x	0	0	1	1	0	1	0		1760 MT/s < f ≤ 1780 MT/s
x	0	0	1	1	0	1	1		1780 MT/s < f ≤ 1800 MT/s
x	0	0	1	1	1	0	0		1800 MT/s < f ≤ 1820 MT/s
x	0	0	1	1	1	0	1		1820 MT/s < f ≤ 1840 MT/s
x	0	0	1	1	1	1	0		1840 MT/s < f ≤ 1860 MT/s
x	0	0	1	1	1	1	1		1860 MT/s < f ≤ 1880 MT/s
x	0	1	0	0	0	0	0		1880 MT/s < f ≤ 1900 MT/s
x	0	1	0	0	0	0	1		1900 MT/s < f ≤ 1920 MT/s
x	0	1	0	0	0	1	0		1920 MT/s < f ≤ 1940 MT/s
x	0	1	0	0	0	1	1		1940 MT/s < f ≤ 1960 MT/s
x	0	1	0	0	1	0	0		1960 MT/s < f ≤ 1980 MT/s
x	0	1	0	0	1	0	1		1980 MT/s < f ≤ 2000 MT/s
x	0	1	0	0	1	1	0		2000 MT/s < f ≤ 2020 MT/s
x	0	1	0	0	1	1	1		2020 MT/s < f ≤ 2040 MT/s
x	0	1	0	1	0	0	0		2040 MT/s < f ≤ 2060 MT/s
x	0	1	0	1	0	0	1		2060 MT/s < f ≤ 2080 MT/s
x	0	1	0	1	0	1	0		2080 MT/s < f ≤ 2100 MT/s
x	0	1	0	1	0	1	1		2100 MT/s < f ≤ 2120 MT/s
x	0	1	0	1	1	0	0		2120 MT/s < f ≤ 2140 MT/s

2.23.21 F0RC3x - Fine Granularity RDIMM Operating Speed

Table 51 — F0RC3x: Fine Granularity RDIMM Operating Speed[1]

Setting (DA[7:0])								Definition	Encoding[2]
x	0	1	0	1	1	0	1		2140 MT/s < f ≤ 2160 MT/s
x	0	1	0	1	1	1	0		2160 MT/s < f ≤ 2180 MT/s
x	0	1	0	1	1	1	1		2180 MT/s < f ≤ 2200 MT/s
x	0	1	1	0	0	0	0		2200 MT/s < f ≤ 2220 MT/s
x	0	1	1	0	0	0	1		2220 MT/s < f ≤ 2240 MT/s
x	0	1	1	0	0	1	0		2240 MT/s < f ≤ 2260 MT/s
x	0	1	1	0	0	1	1		2260 MT/s < f ≤ 2280 MT/s
x	0	1	1	0	1	0	0		2280 MT/s < f ≤ 2300 MT/s
x	0	1	1	0	1	0	1		2300 MT/s < f ≤ 2320 MT/s
x	0	1	1	0	1	1	0		2320 MT/s < f ≤ 2340 MT/s
x	0	1	1	0	1	1	1		2340 MT/s < f ≤ 2360 MT/s
x	0	1	1	1	0	0	0		2360 MT/s < f ≤ 2380 MT/s
x	0	1	1	1	0	0	1		2380 MT/s < f ≤ 2400 MT/s
x	0	1	1	1	0	1	0		2400 MT/s < f ≤ 2420 MT/s
x	0	1	1	1	0	1	1		2420 MT/s < f ≤ 2440 MT/s
x	0	1	1	1	1	0	0		2440 MT/s < f ≤ 2460 MT/s
x	0	1	1	1	1	0	1		2460 MT/s < f ≤ 2480 MT/s
x	0	1	1	1	1	1	0		2480 MT/s < f ≤ 2500 MT/s
x	0	1	1	1	1	1	1		2500 MT/s < f ≤ 2520 MT/s
x	1	0	0	0	0	0	0		2520 MT/s < f ≤ 2540 MT/s
x	1	0	0	0	0	0	1		2540 MT/s < f ≤ 2560 MT/s
x	1	0	0	0	0	1	0		2560 MT/s < f ≤ 2580 MT/s
x	1	0	0	0	0	1	1		2580 MT/s < f ≤ 2600 MT/s
x	1	0	0	0	1	0	0		2600 MT/s < f ≤ 2620 MT/s
x	1	0	0	0	1	0	1		2620 MT/s < f ≤ 2640 MT/s
x	1	0	0	0	1	1	0		2640 MT/s < f ≤ 2660 MT/s
x	1	0	0	0	1	1	1		2660 MT/s < f ≤ 2680 MT/s
x	1	0	0	1	0	0	0		2680 MT/s < f ≤ 2700 MT/s
x	1	0	0	1	0	0	1		2700 MT/s < f ≤ 2720 MT/s
x	1	0	0	1	0	1	0		2720 MT/s < f ≤ 2740 MT/s
x	1	0	0	1	0	1	1		2740 MT/s < f ≤ 2760 MT/s
x	1	0	0	1	1	0	0		2760 MT/s < f ≤ 2780 MT/s
x	1	0	0	1	1	0	1		2780 MT/s < f ≤ 2800 MT/s
x	1	0	0	1	1	1	0		2800 MT/s < f ≤ 2820 MT/s
x	1	0	0	1	1	1	1		2820 MT/s < f ≤ 2840 MT/s
x	1	0	1	0	0	0	0		2840 MT/s < f ≤ 2860 MT/s
x	1	0	1	0	0	0	1		2860 MT/s < f ≤ 2880 MT/s
x	1	0	1	0	0	1	0		2880 MT/s < f ≤ 2900 MT/s
x	1	0	1	0	0	1	1		2900 MT/s < f ≤ 2920 MT/s
x	1	0	1	0	1	0	0		2920 MT/s < f ≤ 2940 MT/s
x	1	0	1	0	1	0	1		2940 MT/s < f ≤ 2960 MT/s
x	1	0	1	0	1	1	0		2960 MT/s < f ≤ 2980 MT/s
x	1	0	1	0	1	1	1		2980 MT/s < f ≤ 3000 MT/s
x	1	0	1	1	0	0	0		3000 MT/s < f ≤ 3020 MT/s
x	1	0	1	1	0	0	1		3020 MT/s < f ≤ 3040 MT/s
x	1	0	1	1	0	1	0		3040 MT/s < f ≤ 3060 MT/s
x	1	0	1	1	0	1	1		3060 MT/s < f ≤ 3080 MT/s
x	1	0	1	1	1	0	0		3080 MT/s < f ≤ 3100 MT/s
x	1	0	1	1	1	0	1		3100 MT/s < f ≤ 3120 MT/s
x	1	0	1	1	1	1	0		3120 MT/s < f ≤ 3140 MT/s
x	1	0	1	1	1	1	1		3140 MT/s < f ≤ 3160 MT/s
x	1	1	0	0	0	0	0		3160 MT/s < f ≤ 3180 MT/s
x	1	1	0	0	0	0	1		3180 MT/s < f ≤ 3200 MT/s
x	1	1	x	x	x	1	x		Reserved
x	1	1	x	x	1	x	x		Reserved
x	1	1	x	1	x	x	x		Reserved
x	1	1	1	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. This control word defines the frequency of the CK_t - CK_c input reference clock during normal operation (i.e., when not in test frequency range) in units of 20 MT/s (i.e., 10 MHz).

2. The frequency ranges shown in this column are for the base frequency of the input clock and they do not include SSC modulation effects. In some cases, due to SSC modulation, the actual frequency of the input clock can straddle two adjacent frequency ranges.
3. The encoding value is used to inform the DDR4RCD02 of the operating speed that it is being run at in a system. It is not an indicator of how fast or slow an RCD can run.
4. The DDR4RCD02 is required to correctly execute RCW Write commands (i.e., DRAM MRS commands) at any valid frequency before the Fine Granularity Operating Speed Control Word is programmed.
5. The host is responsible for programming F0RC3x with the settings corresponding to the input clock frequency before initiating any training procedures with the DRAMs. The host is also responsible for keeping the settings in F0RC3x and F0RC0A consistent with each other.

2.23.22 CW Selection Control Words

Table 52 — F0RC4x: CW Source Selection Control Word

F0RC2x (DA5)[1]	Setting (DA[7:0])								Definition	Encoding
0	0	0	0	A12	A11	A10	A9	A8	Upper CW address for CW Read or CW Write operations	CW read or write to Function space 0 (JEDEC defined)
0	0	0	1	A12	A11	A10	A9	A8		CW read or write to Function space 1 (JEDEC defined)
0	0	1	0	A12	A11	A10	A9	A8		CW read or write to Function space 2 Reserved
0	0	1	1	A12	A11	A10	A9	A8		CW read or write to Function space 3 Reserved
0	1	0	0	A12	A11	A10	A9	A8		CW read or write to Function space 4 Reserved
0	1	0	1	A12	A11	A10	A9	A8		CW read or write to Function space 5 Reserved
0	1	1	0	A12	A11	A10	A9	A8		CW read or write to Function space 6 Reserved
0	1	1	1	A12	A11	A10	A9	A8		CW read or write to Function space 7 Reserved
1	0	0	0	A12	A11	A10	A9	A8	Upper CW address for CW Read or CW Write operation	CW read or write to Function space 8 (vendor specific)
1	0	0	1	A12	A11	A10	A9	A8		CW read or write to Function space 9 (vendor specific)
1	0	1	0	A12	A11	A10	A9	A8		CW read or write to Function space 10 (vendor specific)
1	0	1	1	A12	A11	A10	A9	A8		CW read or write to Function space 11 (vendor specific)
1	1	0	0	A12	A11	A10	A9	A8		CW read or write to Function space 12 (vendor specific)
1	1	0	1	A12	A11	A10	A9	A8		CW read or write to Function space 13 (vendor specific)
1	1	1	0	A12	A11	A10	A9	A8		CW read or write to Function space 14 (vendor specific)
1	1	1	1	A12	A11	A10	A9	A8		CW read or write to Function space 15 (vendor specific)

1. F0RC2x DA5 in F0RC4x only applies when accessing RCD function space and is not used when accessing Data Buffer function spaces.

Table 53 — F0RC5x: CW Destination Selection & Write/Read Additional QxODT[1:0] Signal High Time

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	0	0	Write Operation - Additional QxODT[1:0] High Time to Default Time	Default: 0 nCK addition to QxODT[1:0] High Time
x	x	x	x	x	x	0	1		+1 nCK addition to QxODT[1:0] High Time
x	x	x	x	x	x	1	0		+2 nCK addition to QxODT[1:0] High Time[1]
x	x	x	x	x	x	1	1		Reserved
x	x	x	x	0	0	x	x	Read Operation - Additional QxODT[1:0] High Time to Default Time	Default: 0 nCK addition to QxODT[1:0] High Time
x	x	x	x	0	1	x	x		+1 nCK addition to QxODT[1:0] High Time
x	x	x	x	1	0	x	x		+2 nCK addition to QxODT[1:0] High Time[1]
x	x	x	x	1	1	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
0	MPR bit 1	MPR bit 0	x	x	x	x	x	CW Read or Write Operation[2]	MPR address and AI bit
1	MPR bit 1	MPR bit 0	x	x	x	x	x	CW Read or Write Operation with auto-increment [2,3]	MPR address and AI bit

1. Applicable to 2666 MT/s and higher data rate operation.
2. The MPR bits field (DA[6:5]) bits are only used in CMD4 CW Read Operations and are DON'T CARE for CMD5 CW Write operations
3. CW Read and CW Write commands auto-increment the address field (DA[3:0]) in the CW source selection control F0RC4x word by '1' and the MPR bits field (DA[6:5])in the CW destination selection control word F0RC5x by '1' after the commands are executed. Auto increment is only applicable to 8b CW Reads and CW Writes.

The CW selection control words have to be written before issuing CW Read or CW Write commands. In addition, prior to CW Write commands or prior to accessing 4-bit CWs with a CW Read command, the CW data control word (see Table 54) also has to be written.

2.23.23 CW Data Control Word

Table 54 — F0RC6x: CW Data Control Word

Setting (DA[7:0])								Definition	Encoding
A7	A6	A5	A4	A3	A2	A1	A0	Content of A[7:0] for CW Write or CW Read[1] command	CW data

1. The content of the A[3:0] bits for CW Read commands for 4-bit CWs is DON'T CARE and has no impact on functionality.

The register sends the following bits on it QxA[7:0] outputs for CW Read commands:

Table 55 — CW read command bit assignment for 8-bit CWs

QxA7	QxA6	QxA5	QxA4	QxA3	QxA2	QxA1	QxA0
CW bit 7	CW bit 6	CW bit 5	CW bit 4	CW bit 3	CW bit 2	CW bit 1	CW bit 0

Table 56 — CW read command bit assignment for 4-bit CWs

QxA7	QxA6	QxA5	QxA4	QxA3	QxA2	QxA1	QxA0
Odd address (A4=1) CW bit 3	Odd address (A4=1) CW bit 2	Odd address (A4=1) CW bit 1	Odd address (A4=1) CW bit 0	Even address (A4=0) CW bit 3	Even address (A4=0) CW bit 2	Even address (A4=0) CW bit 1	Even address (A4=0) CW bit 0

The DDR4RCD02 decodes CW Read or CW Write commands with A[11:8] = 0000 in Table 52 as 4-bit commands and all other CW Read or CW Write commands as 8-bit commands.

The RCD will always send two 4-bit CWs on every 4-bit CW Read command. In case of a 4-bit CW Read command

with an even address in F0RC6x DA[7:4], the RCD will send the addressed 4-bit CW on A[3:0] and the next address 4-bit CW on A[7:4]. In case of a 4-bit CW Read command with an odd address in F0RC6x DA[7:4], the RCD will send the addressed 4-bit CW on A[7:4] and the previous address 4-bit CW on A[3:0].

2.23.24 IBT Control Word

Table 57 — F0RC7x: IBT Control Word

Setting (DA[7:0])								Definition[1]	Encoding
x	x	x	x	x	x	0	0	CA Input Bus Termination[2]	100 Ω
x	x	x	x	x	x	0	1		150 Ω
x	x	x	x	x	x	1	0		300 Ω
x	x	x	x	x	x	1	1		OFF
x	x	x	x	0	0	x	x	DCS[3:0]_n Input Bus Termination[3,4]	100 Ω
x	x	x	x	0	1	x	x		150 Ω
x	x	x	x	1	0	x	x		300 Ω
x	x	x	x	1	1	x	x		OFF
x	x	0	0	x	x	x	x	DCKE Input Bus Termination[5]	100 Ω
x	x	0	1	x	x	x	x		150 Ω
x	x	1	0	x	x	x	x		300 Ω
x	x	1	1	x	x	x	x		OFF
0	0	x	x	x	x	x	x	DODT Input Bus Termination[6]	100 Ω
0	1	x	x	x	x	x	x		150 Ω
1	0	x	x	x	x	x	x		300 Ω
1	1	x	x	x	x	x	x		OFF

1. These are target IBT values. Acceptable actual values are determined based on tolerances defined in electrical section.
2. These RCW bits cover the following CA inputs: DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DC2, DPAR
3. These RCW bits cover the following Ctrl inputs: DCS[3:0]_n
4. If the DC[1:0]/DCS[3:2]_n inputs are used for the DC[1:0] function they are not covered by F0RC7x, DA[3:2], but by F0RC7x, DA[1:0] instead
5. These RCW bits cover the following Ctrl inputs: DCKE0, DCKE1
6. These RCW bits cover the following Ctrl inputs: DODT0, DODT1

2.23.25 ODT Input Buffer/IBT, QxODT Output Buffer and Timing Control Word

Table 58 — F0RC8x: ODT Input Buffer/IBT, QxODT Output Buffer and Timing Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	QxODT[1:0] Write Timing[1]	Default: QxODT[1:0] asserted same time as Write command
x	x	x	x	x	x	x	1		QxODT[1:0] assertion 1 nCK after Write command
x	x	x	0	0	0	0	x	QxODT[1:0] Read Timing[1]	Default: QxODT[1:0] asserted same time as Read command
x	x	x	0	0	0	1	x		QxODT[1:0] asserted 1 nCK after Read command
x	x	x	0	0	1	0	x		QxODT[1:0] asserted 2 nCK after Read command
x	x	x	0	0	1	1	x		QxODT[1:0] asserted 3 nCK after Read command
x	x	x	0	1	0	0	x		QxODT[1:0] asserted 4 nCK after Read command
x	x	x	0	1	0	1	x		QxODT[1:0] asserted 5 nCK after Read command
x	x	x	0	1	1	0	x		QxODT[1:0] asserted 6 nCK after Read command
x	x	x	0	1	1	1	x		QxODT[1:0] asserted 7 nCK after Read command
x	x	x	1	0	0	0	x		QxODT[1:0] asserted 8 nCK after Read command
x	x	x	1	0	0	1	x		Reserved
x	x	x	1	0	1	0	x		
x	x	x	1	0	1	1	x		
x	x	x	1	1	0	0	x		
x	x	x	1	1	0	1	x		
x	x	x	1	1	1	0	x		
x	x	x	1	1	1	1	x		

Table 58 — F0RC8x: ODT Input Buffer/IBT, QxODT Output Buffer and Timing Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	0	x	x	x	x	x	BODT Output Driver Disabled	BODT output driver enabled
x	x	1	x	x	x	x	x		BODT output driver disabled[2]
0	0	x	x	x	x	x	x	ODT Input buffer, Output Buffer and IBT Control	Default: Both DODT[1:0] input buffers and IBT are ON and DODT[1:0] inputs are passed to QxODT[1:0] respectively. If F0RC8x DA5 is not set to '1', DODT0 and DODT1 are OR'ed together and the result is passed to BODT.
0	1	x	x	x	x	x	x		DODT0 input buffer and IBT ON and passed to QxODT[0] output. DODT1 input buffer and IBT is OFF and QxODT1 output buffer is OFF. If F0RC8x DA5 is not set to '1', DODT0 is passed to BODT.
1	0	x	x	x	x	x	x		Both DODT[1:0] input buffers and IBT are OFF; QxODT[1:0] outputs are OFF. BODT output is OFF.
1	1	x	x	x	x	x	x		Both DODT[1:0]input buffers and IBT are OFF.; QxODT[1:0] outputs are controlled through F0RC8x bits DA[4:0] for Write and Read timing. F0RC9x for Write Pattern, and F0RCAx for Read Pattern[3]. The BODT output is OFF[2].

1. Only applicable if F0RC8x DA[7:6] = 11. If a parity error is detected with a (Write or Read) command, the RCD may or may not generate the QxODT[1:0] output pulse corresponding to that command.
2. The BODT output driver is disabled. RTT_NOM needs to be disabled in the Data Buffer, which in turn causes the Data Buffer to disable its BODT input receiver.
3. Only applicable if F0RC0F bit DA[2:0] is '000' or '001' or '010' or '011'.

2.23.26 QxODT[1:0] Write Pattern Control Word

Table 59 — F0RC9x[1]: QxODT[1:0] Write Pattern Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	QxODT[0] for Rank 0	Default: QxODT0 Not asserted during Write
x	x	x	x	x	x	x	1		QxODT0 asserted during Write
x	x	x	x	x	x	0	x	QxODT[1] for Rank 0	Default: QxODT1 Not asserted during Write
x	x	x	x	x	x	1	x		QxODT1 asserted during Write
x	x	x	x	x	0	x	x	QxODT[0] for Rank 1	Default: QxODT0 Not asserted during Write
x	x	x	x	x	1	x	x		QxODT0 asserted during Write
x	x	x	x	0	x	x	x	QxODT[1] for Rank 1	Default: QxODT1 Not asserted during Write
x	x	x	x	1	x	x	x		QxODT1 asserted during Write
x	x	x	0	x	x	x	x	QxODT[0] for Rank 2	Default: QxODT0 Not asserted during Write
x	x	x	1	x	x	x	x		QxODT0 asserted during Write
x	x	0	x	x	x	x	x	QxODT[1] for Rank 2	Default: QxODT1 Not asserted during Write
x	x	1	x	x	x	x	x		QxODT1 asserted during Write
x	0	x	x	x	x	x	x	QxODT[0] for Rank 3	Default: QxODT0 Not asserted during Write
x	1	x	x	x	x	x	x		QxODT0 asserted during Write
0	x	x	x	x	x	x	x	QxODT[1] for Rank 3	Default: QxODT1 Not asserted during Write
1	x	x	x	x	x	x	x		QxODT1 asserted during Write

1. -Only applicable if F0RC8x DA[7:6] = 11

2.23.27 QxODT[1:0] Read Pattern Control Word

Table 60 — F0RCAx[1]: QxODT[1:0] Read Pattern Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	QxODT[0] for Rank 0	Default: QxODT0 Not asserted during Read
x	x	x	x	x	x	x	1		QxODT0 asserted during Read
x	x	x	x	x	x	0	x	QxODT[1] for Rank 0	Default: QxODT1 Not asserted during Read
x	x	x	x	x	x	1	x		QxODT1 asserted during Read
x	x	x	x	x	0	x	x	QxODT[0] for Rank 1	Default: QxODT0 Not asserted during Read
x	x	x	x	x	1	x	x		QxODT0 asserted during Read
x	x	x	x	0	x	x	x	QxODT[1] for Rank 1	Default: QxODT1 Not asserted during Read
x	x	x	x	1	x	x	x		QxODT1 asserted during Read
x	x	x	0	x	x	x	x	QxODT[0] for Rank 2	Default: QxODT0 Not asserted during Read
x	x	x	1	x	x	x	x		QxODT0 asserted during Read
x	x	0	x	x	x	x	x	QxODT[1] for Rank 2	Default: QxODT1 Not asserted during Read
x	x	1	x	x	x	x	x		QxODT1 asserted during Read
x	0	x	x	x	x	x	x	QxODT[0] for Rank 3	Default: QxODT0 Not asserted during Read
x	1	x	x	x	x	x	x		QxODT0 asserted during Read
0	x	x	x	x	x	x	x	QxODT[1] for Rank 3	Default: QxODT1 Not asserted during Read
1	x	x	x	x	x	x	x		QxODT1 asserted during Read

1. Only applicable if F0RC8x DA[7:6] = 11

2.23.28 IBT and MRS Snoop Control Word

Table 61 — F0RCBx: IBT and MRS Snoop Control Word[1]

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	DC0 Input Bus Termination Disable	Enabled
x	x	x	x	x	x	x	1		Disabled
x	x	x	x	x	x	0	x	DC1 Input Bus Termination Disable	Enabled
x	x	x	x	x	x	1	x		Disabled
x	x	x	x	x	0	x	x	DC2 Input Bus Termination Disable	Enabled
x	x	x	x	x	1	x	x		Disabled
x	x	x	x	0	x	x	x	DDR4DB02 MRS Snoop Disable	Enabled[2]
x	x	x	x	1	x	x	x		Disabled[3]
x	x	x	0	x	x	x	x	DDR4RCD02 MRS Snoop Disable	Enabled[4]
x	x	x	1	x	x	x	x		Disabled[5]
x	x	0	x	x	x	x	x	DCKE1 Input Bus Termination Disable	Enabled
x	x	1	x	x	x	x	x		Disabled
x	0	x	x	x	x	x	x	DCKE1 Input Buffer and QxCKE1 Output Driver Disable	Enabled
x	1	x	x	x	x	x	x		Disabled[6]
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. RCD always snoops DRAM MRS command for Write/Read Preamble, Burst Length and Write CRC if F0RC8X DA[7:6] = 11.
2. If LRDIMM is enabled and F0RCBx DA3 = 0, MRS commands for DRAM MR[6:0] to Rank 0, A-side received by the DDR4RCD02 results in MRS WR command on the BCOM bus.
3. If LRDIMM is enabled and F0RCBx DA3 = 1, MRS commands for DRAM MR[6:0] to the DDR4RCD02 results in NOP command on the BCOM bus. This mode requires that the host explicitly writes to the DDR4DB02 snoop register BCWs.
4. If LRDIMM is enabled and F0RCBx DA4 = 0, the DDR4RCD02 will snoop information from MRS commands for DRAM MR[6:0] as needed for its own use.
5. If LRDIMM is enabled and F0RCBx DA4 = 1, the DDR4RCD02 will not snoop information from MRS commands for DRAM MR[6:0] for its own use. This mode requires that the host explicitly sets the snoop bits in the DDR4RCD02.
6. When the input buffer is disabled, the DCKE1 input signal is assumed to be LOW by internal logic in the DDR4RCD02 If F0RC9x DA3 = 1 then the RCD will enter CKE power down state when host drives DCKE0 Low.

2.23.29 F0RCCx .. F0RCFFx - Error Log Register

The control word locations Cx .. Fx function as a 32-bit error log register. Upon occurrence of a CA parity error the device logs the following sampled command and address bits in the Error Log Register, which can be transferred by the memory controller to page 0 of the DRAM MPR, where it can be read by the host.

Table 62 — F0RCCx .. F0RCFx: Error Log Register[1]

Control Word	Setting (DA[7:0])							
F0RCCx	A7	A6	A5	A4	A3	A2	A1	A0
F0RCDx	A15/ CAS_n	A14/ WE_n	A13	A12	A11	A10	A9	A8
F0RCEx	DPAR	ACT_n	BG1	BG0	BA1	BA0	A17	A16/ RAS_n
F0RCFx	> 1 Error[2,3]	CA Parity Error Status[2,4]	Reserved	CS1_n	CS0_n	C2	C1/ CS3_n	C0/ CS2_n

1. When command and address bits are logged in the Error Log Register upon occurrence of a CA parity error, all bits in F0RCCx/Dx/Ex(DA[7:0]) and in F0RCFx(DA[4:0]) are updated with the corresponding values from the offending command.
2. This bit will get reset to '0' when "Clear CA Parity Error" command is sent. The Clear CA Parity Error command does not affect any bits in F0RCCx/Dx/Ex and it does not affect Bits DA[2:0] in F0RCFx.
3. With F0RC0E DA3 = 1 and DA2 = 1 the device will forward commands and re-enable parity after the ALERT_n pulse. The CA Parity Error Status bit will remain set. If a subsequent parity error is detected the device will re-enter the parity error state and set the '> 1 Error' bit.
4. The DDR4RCD02 will set this bit upon occurrence of a CA parity error.

2.23.30 F1RC00 - Data Buffer Interface Driver Characteristics Control Word

Table 63 — F1RC00: Data Buffer Interface Driver Characteristics Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	BCOM[3:0], BODT, BCKE, driver strength	Moderate Drive
x	x	x	1		Strong Drive
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
x	0	x	x	BCK_t/BCK_c driver strength	Moderate Drive
x	1	x	x		Strong Drive
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

2.23.31 F1RC01 - CAL Mode Snoop Enable

Table 64 — F1RC01: CAL Mode Snoop enable

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	CAL mode snooping enable	Snoop Disabled
x	x	x	1		Snoop Enabled
x	x	0	x	Reserved	Reserved
x	x	1	x		Reserved
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

2.23.32 F1RC02 - CA and CS Output Slew Rate Control

Table 65 — F1RC02: CA and CS Output Slew Rate Control[1]

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	Slew rate control for Address/ Command - QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR, QxC0[2] QxC1[2]	(Default) Moderate: Single-ended range 3 V/ns - 6 V/ns
x	x	0	1		Fast: Single-ended range 5 V/ns - 8 V/ns
x	x	1	0		Slow: Single-ended range 2 V/ns - 4 V/ns
x	x	1	1		Reserved
0	0	x	x	QxCS0_n, QxCS1_n, QxCS2_n[2],QxCS3_n[2] Outputs	(Default) Moderate: Single-ended 3 V/ns - 6 V/ns
0	1	x	x		Fast: Single-ended range 5 V/ns - 8 V/ns
1	0	x	x		Slow: Single-ended range 2 V/ns - 4 V/ns
1	1	x	x		Reserved

1. Slew Rate Control encodings of Moderate, Fast and Slow apply to all driver strength settings. The base range values specified in Table 65 are applicable for Ron = RZQ/24, VDD = 1.2 V and 25 °C. The Output slew rate is verified by design and characterization, and may not be subject to production test.
2. If QxC0/CS2_n and QxC1/CS3_n are configured as QxC0 and QxC1 then output slew rates are defined by F1RC02 DA[1:0]. If QxC0/CS2_n and QxC1/CS3_n are configured as QxC2S_n and QxCS3_n then output slew rates are defined by F1RC02 DA[3:2].

2.23.33 F1RC03 - ODT and CKEn Output Slew Rate Control

Table 66 — F1RC03: ODT and CKE Output Slew Rate Control

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	Slew rate control for QxODT0 .. QxODT1 output drivers [1]	(Default) Moderate: Single-ended range 3 V/ns - 6 V/ns
x	x	0	1		Fast: Single-ended range 5 V/ns - 8 V/ns
x	x	1	0		Slow: Single-ended range 2 V/ns - 4 V/ns
x	x	1	1		Reserved
0	0	x	x	Slew rate control for QxCKE0 .. QxCKE1 output drivers [1]	(Default) Moderate: Single-ended range 3 V/ns - 6 V/ns
0	1	x	x		Fast: Single-ended range 5 V/ns - 8 V/ns
1	0	x	x		Slow: Single-ended range 2 V/ns - 4 V/ns
1	1	x	x		Reserved

1. Slew Rate Control encodings of Moderate, Fast and Slow apply to all driver strength settings. The base range values specified in Table 66 are applicable for Ron = RZQ/24, VDD = 1.2 V and 25 °C. The Output slew rate is verified by design and characterization, and may not be subject to production test.

2.23.34 F1RC04 - Clock Driver Output Slew Rate Control

Table 67 — F1RC04: Clock Driver Output Slew Rate Control

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	Slew rate control for Clock Y1_t, Y1_c, Y3_t, and Y3_c differential output drivers (A side) [1]	(Default) Moderate: Differential range 6 V/ns - 12 V/ns
x	x	0	1		Fast: Differential range 10 V/ns -16 V/ns
x	x	1	0		Slow: Differential range 4 V/ns - 8 V/ns
x	x	1	1		Reserved
0	0	x	x	Slew rate control for Clock Y0_t, Y0_c, Y2_t, and Y2_c differential output drivers (B side) [1]	(Default) Moderate: Differential range 6 V/ns - 12V/ns
0	1	x	x		Fast: Differential range 10 V/ns - 16 V/ns
1	0	x	x		Slow: Differential range 4 V/ns - 8 V/ns
1	1	x	x		Reserved

1. Slew Rate Control encodings of Moderate, Fast and Slow apply to all driver strength settings. The base range values specified in Table 67 are applicable for Ron = RZQ/24, VDD = 1.2 V and 25 °C.The Output slew rate is verified by design and characterization, and may not be subject to production test.

2.23.35 F1RC05 - Data Buffer Interface Output Slew Rate Control

Table 68 — F1RC05: Data Buffer Interface Output Slew Rate Control

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	Slew rate control for BCOM[3:0], BODT, BCKE output drivers [1]	(Default) Moderate: Single-ended range 3 V/ns - 6 V/ns
x	x	0	1		Fast: Single-ended range 5 V/ns - 8 V/ns
x	x	1	0		Slow: Single-ended range 2 V/ns - 4 V/ns
x	x	1	1		Reserved
0	0	x	x	Slew rate control for BCK_t, BCK_c differential output drivers [1]	(Default) Moderate: Differential range 6 V/ns - 12 V/ns
0	1	x	x		Fast: Differential range 10 V/ns - 16 V/ns
1	0	x	x		Slow: Differential range 4 V/ns - 8 V/ns
1	1	x	x		Reserved

1. Slew Rate Control encodings of Moderate, Fast and Slow apply to all driver strength settings. The base range values specified in Table 68 are applicable for Ron = RZQ/17, VDD = 1.2 V and 25 °C. The Output slew rate is verified by design and characterization, and may not be subject to production test.

2.23.36 F1RC1x - QxCSn_n Output Delay Control Word

Table 69 — F1RC1x: QxCSn_n Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Output Delay Control for QACS0_n, QACS1_n, QBCS0_n, and QBCS1_n Output Signals1 [1]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	x	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	x	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	x	...						
x	x	x	1	1	1	0	1		Delay Outputs by +(29/64) * t_{CK}
x	x	x	1	1	1	1	0		Delay Outputs by +(30/64) * t_{CK}
x	x	x	1	1	1	1	1		Delay Outputs by +(31/64) * t_{CK}
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QACS0_n, QACS1_n and QBCS0_n, and QBCS1_n	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled [2]

1. These control bits do not have any effect unless F1RC1x DA7 = 1.
2. When feature is enabled the delay settings in F1RC1x require a time of t_{ODU} for the delay to become stable on the outputs.

2.23.37 F1RC2x - QxCn Output Delay Control Word

Table 70 — F1RC2x: QxCn Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Output Delay Control for QAC0/CS2_n , QBC0/CS2_n, QAC1/ CS3_n , and QBC1/CS3_n Output Signals [1]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	x	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	x	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	x	...						
x	x	x	1	1	1	0	1		Delay Outputs by +(29/64) * t_{CK}
x	x	x	1	1	1	1	0		Delay Outputs by +(30/64) * t_{CK}
x	x	x	1	1	1	1	1		Delay Outputs by +(31/64) * t_{CK}
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QAC0/CS2_n , QBC0/CS2_n, QAC1/ CS3_n , and QBC1/CS3_n	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled [2]

1. These control bits do not have any effect unless F1RC2x DA7 = 1.
2. When feature is enabled the delay settings in F1RC2x require a time of t_{ODU} for the delay to become stable on the outputs.

2.23.38 F1RC3x - QxCKEn Output Delay Control Word

Table 71 — F1RC3x: QxCKEn Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Output Delay Control for QACKE0, QBCKE0, QACKE1 and QBCKE1 Output Signals[1]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	x	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	x	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	x	...						
x	x	x	1	1	1	0	1		Delay Outputs by +(29/64) * t_{CK}
x	x	x	1	1	1	1	0		Delay Outputs by +(30/64) * t_{CK}
x	x	x	1	1	1	1	1		Delay Outputs by +(31/64) * t_{CK}
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QACKE0, QBCKE0, QACKE1 and QBCKE1	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[2]

1. These control bits do not have any effect unless F1RC3x DA7 = 1.
2. When feature is enabled the delay settings in F1RC3x require a time of t_{ODU} for the delay to become stable on the outputs.

2.23.39 F1RC4x - QxODTn Output Delay Control Word

Table 72 — F1RC4x: QxODTn Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Output Delay Control for QAODT0, QBODT0, QAODT1, and QBODT1 Output Signals[1]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	x	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	x	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	x	...						
x	x	x	1	1	1	0	1		Delay Outputs by +(29/64) * t_{CK}
x	x	x	1	1	1	1	0		Delay Outputs by +(30/64) * t_{CK}
x	x	x	1	1	1	1	1		Delay Outputs by +(31/64) * t_{CK}
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QAODT0, QBODT0, QAODT1, and QBODT1	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[2]

1. These control bits do not have any effect unless F1RC4x DA7 = 1.
2. When feature is enabled the delay settings in F1RC4x require a time of t_{ODU} for the delay to become stable on the outputs.

2.23.40 F1RC5x - QxCA Output Delay Control Word

Table 73 — F1RC5x: QxCA Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Output Delay Control for QACMD/ ADD and QBCMD/ADD[1] Output Signals[2]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	x	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	x	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	x	...						
x	x	x	1	1	1	0	1		Delay Outputs by +(29/64) * t_{CK}
x	x	x	1	1	1	1	0		Delay Outputs by +(30/64) * t_{CK}
x	x	x	1	1	1	1	1		Delay Outputs by +(31/64) * t_{CK}
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for QACMD/ADD and QBCMD/ADD	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[3]

1. These control bits apply to the following CA outputs: QAA0..QAA17, QABA0..QABA1, QABG0..QABG1, QAACT_n, QAC2, and QAPAR, QBA0..QBA17, QBBA0..QBBA1, QBBG0..QBBG1, QBACT_n, QBC2, and QBPAR.
2. These control bits do not have any effect unless F1RC5x DA7 = 1.
3. When feature is enabled the delay settings in F1RC5x require a time of t_{ODU} for the delay to become stable on the outputs.

2.23.41 F1RC6x - Y1/Y3 Output Delay Control Word

Table 74 — F1RC6x: Y1/Y3 Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	0	0	0	0	0	0	Output Delay Control for Y1_t/ Y1_c and Y3_t/Y3_c Output Signals[1]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64)* t_{CK}
x	x	0	...						
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for Y1_t/Y1_c and Y3_t/Y3_c	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[2]

1. These control bits do not have any effect unless F1RC6x DA7 = 1.
2. When feature is enabled the delay settings in F1RC6x require a time of t_{ODU} for the delay to become stable on the outputs.

2.23.42 F1RC7x: Y0/Y2 Output Delay Control Word

Table 75 — F1RC7x: Y0/Y2 Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	0	0	0	0	0	0	Output Delay Control for Y0_t/Y0_c and Y2_t/Y2_c Output Signals[1]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	0	...						
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for Y0_t/Y0_c and Y2_t/Y2_c	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[2]

1. These control bits do not have any effect unless F1RC7x DA7 = 1.

2.When feature is enabled the delay settings in F1RC7x require a time of t_{ODU} for the delay to become stable on the outputs.

2.23.43 F1RC8x: BCOM[3:0]/BCKE/BODT Output Delay Control Word

Table 76 — F1RC8x: BCOM[3:0]/BCKE/BODT Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	0	0	0	0	0	Output Delay Control for BCOM[3:0], BCKE and BODT Output Signals[1]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	x	0	0	0	0	1		Delay Outputs by +(1/64)* t_{CK}
x	x	x	0	0	0	1	0		Delay Outputs by +(2/64) * t_{CK}
x	x	x	...						
x	x	x	1	1	1	0	1		Delay Outputs by +(29/64) * t_{CK}
x	x	x	1	1	1	1	0		Delay Outputs by +(30/64) * t_{CK}
x	x	x	1	1	1	1	1		Delay Outputs by +(31/64) * t_{CK}
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for BCOM[3:0], BCKE and BODT	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[2]

1. These control bits do not have any effect unless F1RC8x DA7 = 1.
2. When feature is enabled the delay settings in F1RC8x require a time of t_{ODU} for the delay to become stable on the outputs.

2.23.44 F1RC9x: BCK Output Delay Control Word

Table 77 — F1RC9x: BCK Output Delay Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	0	0	0	0	0	0	Output Delay Control for BCK_t/BCK_c Output Signals[1]	Delay Outputs by +(0/64) * t_{CK} (Same as Default)
x	x	0	0	0	0	0	1		Delay Outputs by +(1/64) * t_{CK}
x	x	0	0	0	0	1	0		Delay Outputs by +(2/64)* t_{CK}
x	x	0	0	0	0	1	1		Delay Outputs by +(3/64) * t_{CK}
x	x	0	...						
x	x	1	1	1	1	0	1		Delay Outputs by +(61/64) * t_{CK}
x	x	1	1	1	1	1	0		Delay Outputs by +(62/64) * t_{CK}
x	x	1	1	1	1	1	1		Delay Outputs by +(63/64) * t_{CK}
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Output Delay Feature Enable for BCK_t/BCK_c	(Default) Feature Disabled
1	x	x	x	x	x	x	x		Feature Enabled[2]

1. These control bits do not have any effect unless F1RC9x DA7 = 1.
2. When feature is enabled the delay settings in F1RC9x require a time of t_{ODU} for the delay to become stable on the outputs.

2.23.45 F4RC00 - NVDIMM Mode Enable Control Word

If the optional NVDIMM mode feature is supported, control word F4RC00 must be implemented. When F4RC00 - DA0 is set to 1 (NVDIMM mode enabled) control word F4RC00 can only be written through the LCOM[2:0] interface regardless of the settings programmed in F4RC00 - DA[2:1]. When F4RC00 - DA0 = 1, F4RC00 cannot be accessed for reads or writes through the Host CTRL/CMD/ADD or I^2C interfaces (i.e., it will be treated as a reserved location).

Table 78 — F4RC00: NVDIMM Mode Enable Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	NVDIMM Mode Enable[1]	(Default) NVDIMM Mode Disabled[2]
x	x	x	1		NVDIMM Mode Enabled[3]
x	x	0	x	LCK_t/LCK_c Input Clock Selection[4]	(Default) LCK_t/LCK_c to LCOM interface only[5]
x	x	1	x		LCK_t/LCK_c controls RCD02 outputs[6,7]
x	0	x	x	Host CTRL/CMD/ADD Interface Selection[8]	(Default) Host CTRL/CMD/ADD inputs enabled
x	1	x	x		Host CTRL/CMD/ADD inputs ignored[9]
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

1. It is expected the Host controller will program this control bit during the initialization sequence. The setting in this control bit is not expected to change after system initialization is complete. This control bit can only be modified when the NV Mode Enable Lock bit in F0RC0E - DA1 is equal to '0'
2. Normal RDIMM or LRDIMM operation with NVDIMM features disabled. Shared pins (i.e., Y2_t/LCOM1, Y2_c/LCOM0, Y3_t/LCK_t, and Y3_c/LCK_c) assume their normal mode functions. No commands or status data can be transferred through the LCOM[2:0] interface. Input LCKE is ignored.
3. NVDIMM operation enabled. Shared pins (i.e., Y2_t/LCOM1, Y2_c/LCOM0, Y3_t/LCK_t, and Y3_c/LCK_c) assume their NVDIMM mode functions and input LCKE is enabled. The DDR4RCD02 ignores Host interface CTRL/CMD/ADD signals when F4RC00 Bits DA1 or DA2 are set to 1
4. This control bit has no effect when NVDIMM features are disabled by F4RC00 - DA0. When PLL reference control is transferred between PLL shutdown and CK_t/CK_c clocks, the RCD02 hardware is responsible for triggering a PLL locking procedure, and the user is responsible for providing a valid input clock signal that meets the t_{ACT} parameter (16 clock cycles) on the enabled clock input receiver and waiting for the PLL to stabilize (t_{STAB}).
5. When F4RC00 - DA1 is 0 the LCK_t/LCK_c clock input is only used for synchronizing command frame and read data frame bit updates on the LCOM[1:0] signals and the CK_t/CK_c input and clock stop detection circuits are active. DRAM and Data Buffer commands are not supported on the LCOM[2:0] interface in this case. Only RCW Write commands are supported by the LCOM[2:0] interface and CMD/ADD/CTRL outputs are controlled by CMD/ADD/CTRL inputs from the Host interface.
6. When F4RC00 - DA1 is set to 1 the LCK_t/LCK_c clock and LCOM[2:0] bus control the RCD02 outputs and CMD/ADD/CTRL inputs from the Host interface are disabled and the signals connected to those inputs are ignored.
7. The RCD02 is responsible for resetting the I^2C interface state machine upon detecting SCL low for 35 ms cumulative between the Start and Stop bits or detecting SCL high continuously for 100 µs. Scaling of the SCL reset timing described in the "I^2C Interface State Machine Reset" section does not apply while the LCK_t/LCK_c clock input has full control the RCD02 device.
8. This control bit has no effect on RCD02 CK_t/CK_c input.
9. To ensure a seamless transition, it is expected that F4RC00 - DA2 will be written to 1 when F4RC00 - DA1 is still 0. In this case, QxCS[i:0]_n outputs will be driven HIGH (i.e., Deselect command will be sent to all DRAMs), QxCKE[1:0] and BCKE outputs will retain their previous values statically, QxODT[1:0] and BODT outputs will drive LOW. and CMD/ADD outputs will drive static HIGH or LOW logic levels to DRAMs unless QxCKE[1:0] output signals are all LOW and CKE Power Down mode is enabled (F0RC09 - DA3 = 1), in which case the CMD/ADD outputs will continue to be disabled.

2.23.46 F4RC01 - NVDIMM Asynchronous Interrupt Control Word

If the optional NVDIMM mode feature is supported, control word F4RC01 must be implemented.

Table 79 — F4RC01: NVDIMM Asynchronous Interrupt Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	x	0	LCOM0 Asynchronous Interrupt Control[1]	(Default) LCOM0 driven LOW
x	x	x	1		LCOM0 driven HIGH
x	x	0	x	LCOM1 Asynchronous Interrupt Control[2]	(Default) LCOM1 driven LOW
x	x	1	x		LCOM1 driven HIGH
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

1. This control bit defines the logic level driven on the LCOM0 output when LCKE is LOW and there is no active RCW read data transfer.
2. This control bit defines the logic level driven on the LCOM1 output when LCKE is LOW and there is no active RCW read data transfer.

2.23.47 F4RC02 - Read Frame Gear Ratio and Yn/BCK Frequency Ratio Control Word

If the optional NVDIMM mode feature is supported, control word F4RC02 must be implemented. When F4RC00 - DA0 is set to 1 (NVDIMM mode enabled) the F4RC02 control word can only be written through the LCOM[2:0] interface regardless of the settings programmed in F4RC00 - DA[2:1]. When F4RC00 - DA0 = 1, F4RC02 cannot be accessed for reads or writes through the Host CTRL/CMD/ADD or I^2C interfaces (i.e., it will be treated as a reserved location).

Table 80 — F4RC02: Read Frame Gear Ratio and Yn/BCK Frequency Ratio Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	Read Frame Data Gear Ratio Control[1]	(Default) Gear ratio = 2
x	x	0	1		Gear ratio = 4
x	x	1	0		Reserved
x	x	1	1		Gear ratio = 1
0	0	x	x	LCK_t/LCK_c to Yn/BCK Clock Ratio Selection[2]	(Default) Yn/BCK frequency = 8 x LCK freq.[3]
0	1	x	x		Reserved
1	0	x	x		Yn/BCK frequency = (1/4) x LCK freq.[4]
1	1	x	x		Reserved

1. This field defines the number of LCK clock cycles used to transfer each bit of RCW data in the read data frame. For example, setting '01' in this field means that each bit of read data is driven by the RCD02 on the LCOM[1:0] pins during four cycles of the LCK clock.
2. This control field has no effect when NVDIMM features are disabled by F4RC00 - DA0 and it has no effect unless F4RC00 Bit DA1 is set to 1.
3. This mode is intended for support of LRDIMM-based NVDIMM modules with DRAMs running in "DLL on" mode at 800 MHz (DDR4-1600), 933 MHz (DDR4-1866), 1066 MHz (DDR4-2133), 1200 MHz (DDR4-2400), 1333 MHz (DDR4-2666), 1466 MHz (DDR4-2933) and 1600 MHz (DDR4-3200). LCK controls the PLL in this case.
4. This mode is intended for support of RDIMM-based NVDIMM modules with DRAMs running in "DLL off" mode at any frequency between 10 MHz and 125 MHz.

2.23.48 F4RC03 – LCOM Receiver Termination Control Word

Optional NVDIMM support feature. F4RC03 controls the receiver termination as shown in Table 81.

Table 81 — F4RC03: LCOM Receiver Termination Control Word

Setting (DA[3:0])				Definition	Encoding
x	x	0	0	Input Termination for LCKE, LCOM[2] and LCOM[1:0][1]	50W termination. Use with Vref[2] = 0.75 * V_{DD}
x	x	0	1		100W termination. Use with Vref[2] = 0.65 * V_{DD}
x	x	1	0		Unterminated. Use with Vref[2] = 0. 50 * V_{DD}
x	x	1	1		Reserved
x	0	x	x	Reserved	Reserved
x	1	x	x		Reserved
0	x	x	x	Reserved	Reserved
1	x	x	x		Reserved

1. These are the termination values. Acceptable actual values are determined based on the tolerance defined in the electrical section.
2. Set the Vref options in F4RC04

2.23.49 F4RC04 – LCOM Receiver Vref Control Word

Optional NVDIMM support feature. F4RC04 controls the receiver Vref trim as shown in Table 82.

Table 82 — F4RC04: LCOM Receiver Vref Control Word

Setting (DA[3:0])				LCOM Vref	Encoding
0	0	0	0	0.50 * V_{DD}	Required. Use with unterminated[1, 2]
0	0	0	1	0.55 * V_{DD}	Optional
0	0	1	0	0.60 * V_{DD}	Optional
0	0	1	1	0.65 * V_{DD}	Required. Use with 100Ω termination[1, 2]
0	1	0	0	0.70 * V_{DD}	Optional
0	1	0	1	0.75 * V_{DD}	Default Setting. Required. Use with 50Ω termination[1, 2]
0	1	1	0	0.80 * V_{DD}	Optional
0	1	1	1	0.85 * V_{DD}	Optional
1	x	x	x	Reserved	Reserved

1. Assumption: the NVC driver RON is 50Ω
2. Set the corresponding termination value in F4RC03

2.23.50 F4RC1x .. F4RC4x - Multi Purpose Registers

If the optional NVDIMM mode feature is supported, control words F4RC1x .. F4RC4x must be implemented. Control word locations F4RC1x .. F4RC4x contain general purpose control bit settings intended for in-band transfer of commands or data from the Host controller to the NVC. The contents of these control words have no effect on the RCD02 device. When F4RC00 - DA[2:0] = '001', Control Words F4RC1x .. F4RC4x can only be written by the Host controller and they can only be read through the LCOM[2:0] interface.

Table 83 — F4RC1x .. F4RC4x: Multi Purpose Registers

Control Word	Setting (DA[7:4])	Setting (DA[3:0])
F4RC1x (DA[7:0]) = MPR0	General purpose in-band control bits (default value = 0101)	General purpose in-band control bits (default value = 0101)
F4RC2x (DA[7:0]) = MPR1	General purpose in-band control bits (default value = 0011)	General purpose in-band control bits (default value = 0011)
F4RC3x (DA[7:0]) = MPR2	General purpose in-band control bits (default value = 0000)	General purpose in-band control bits (default value = 1111)
F4RC4x (DA[7:0]) = MPR3	General purpose in-band control bits (default value = 0000)	General purpose in-band control bits (default value = 0000)

2.23.51 F4RC5x - Data Transfer (Copy and Restore) Control Word

If the optional NVDIMM mode feature is supported, control word F4RC5x must be implemented. Control Word F4RC5x is intended for use of the NVDIMM local controller device. The settings contained in F4RC5x are not used by the RCD02 device. The Host controller can use the asynchronous interrupt feature (F4RC01) when LCKE is LOW to give an indication to the NVC that it needs to execute a new command in F4RC5x.

Table 84 — F4RC5x: Data Transfer (Copy and Restore) Control Word

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	0	0	0	NVDIMM DRAM Logical Rank Selection – Logical Rank 0 to7	(Default) Logical Rank 0
x	x	x	x	x	0	0	1		Logical Rank 1
x	x	x	x	x	...				...
x	x	x	x	x	1	1	0		Logical Rank 6
x	x	x	x	x	1	1	1		Logical Rank 7
x	x	0	0	0	x	x	x	NVDIMM Flash Copy (if more than 1)	(Default) Copy 0
x	x	0	0	1	x	x	x		Copy 1
x	x	...			x	x	x		...
x	x	1	1	0	x	x	x		Copy 6
x	x	1	1	1	x	x	x		Copy 7
x	0	x	x	x	x	x	x	Logical Rank Mode	(Default) Rank specified in DA[2:0]/DA[5:3]
x	1	x	x	x	x	x	x		All logical Ranks; Ignore DA[2:0] /DA[5:3]
0	x	x	x	x	x	x	x	Transfer Type Selection	(Default) Copy Data from DRAM to Flash
1	x	x	x	x	x	x	x		Restore Data from Flash to DRAM

2.23.52 F4RC6x: Self Refresh Status Word

Optional NVDIMM support feature. The DDR4RCD02 tracks self-refresh commands issued by the host interface to DRAM ranks associated with each CKE. This RCW indicates the expected DRAM state based on the sequence of commands issued.

Table 85 — F4RC6x: Self-Refresh StatusWord

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	x	x	x	0	RCD detection of SRE commands[1]	SRE not detected for CKE0 rank or ranks[2]
x	x	x	x	x	x	x	1		SRE detected for CKE0 rank or ranks [3]
x	x	x	x	x	x	0	x		SRE not detected for CKE1 rank or ranks[2]
x	x	x	x	x	x	1	x		SRE detected for CKE0 rank or ranks
x	x	x	x	x	0	x	x	Reserved	Reserved
x	x	x	x	x	1	x	x		Reserved
x	x	x	x	0	x	x	x	Reserved	Reserved
x	x	x	x	1	x	x	x		Reserved
x	x	x	0	x	x	x	x	Reserved	Reserved
x	x	x	1	x	x	x	x		Reserved
x	x	0	x	x	x	x	x	Reserved	Reserved
x	x	1	x	x	x	x	x		Reserved
x	0	x	x	x	x	x	x	Reserved	Reserved
x	1	x	x	x	x	x	x		Reserved
0	x	x	x	x	x	x	x	Reserved	Reserved
1	x	x	x	x	x	x	x		Reserved

1. These bits are read only.
2. State is set to 0 when any of the following conditions is true:
   - Host command is not SRE
   - DCKEx is asserted
   - Host issues SRE command with a parity error
   - Host issues SRE command that causes ERROR_IN is asserted
3. DDR4RCD02 sets state to 1 when host issues SRE command with no parity error and ERROR_IN is not asserted

2.23.53 F7RC1x - Date Code Byte 0

Manufacturing Information Register

Table 86 — F7RC1x: Date Code Byte 0

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Date Code Digit 0[1,2] Year Information	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 1[1,2] Year Information	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

1. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.

2. This is year date code byte for RCD. It must be represented in Binary Coded Decimal (BCD). For example, year 2015 would be coded as 0x15 (0001 0101).

2.23.54 F7RC2x - Date Code Byte 1

Manufacturing Information Register

Table 87 — F7RC2x: Date Code Byte 1

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Date Code Digit 2[1,2] Work Week Information	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 3[1,2] Work Week Information	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

1. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.
2. This is work week date code byte for RCD. It must be represented in Binary Coded Decimal (BCD). For example, week 47 would be coded as 0x47 (0100 0111).

2.23.55 F7RC3x - Date Code Byte 2

Manufacturing Information Register

Table 88 — F7RC3x: Date Code Byte 2

Setting (DA[7:0])								Definition	Encoding
x	x	x	x	0	0	0	0	Date Code Digit 4[1] Reserved	Digit = 0
x	x	x	x	0	0	0	1		Digit = 1
x	x	x	x	0	0	1	0		Digit = 2
x	x	x	x	...					...
x	x	x	x	0	1	1	1		Digit = 7
x	x	x	x	1	0	0	0		Digit = 8
x	x	x	x	1	0	0	1		Digit = 9
x	x	x	x	1	0	1	0		Codes 10 to 15 Reserved
x	x	x	x	...					
x	x	x	x	1	1	1	1		
0	0	0	0	x	x	x	x	Date Code Digit 5[1] Reserved	Digit = 0
0	0	0	1	x	x	x	x		Digit = 1
0	0	1	0	x	x	x	x		Digit = 2
...				x	x	x	x		...
0	1	1	1	x	x	x	x		Digit = 7
1	0	0	0	x	x	x	x		Digit = 8
1	0	0	1	x	x	x	x		Digit = 9
1	0	1	0	x	x	x	x		Codes 10 to 15 Reserved
...				x	x	x	x		
1	1	1	1	x	x	x	x		

1. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.

2.23.56 F7RC4x - Vendor Specific Unique Unit Code Byte 0

Manufacturing Information Register

Table 89 — F7RC4x: Vendor Specific Unique Unit Code Byte 0

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 0 of Unique Unit Code[1]	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.

2.23.57 F7RC5x - Vendor Specific Unique Unit Code Byte 1

Manufacturing Information Register

Table 90 — F7RC5x: Vendor Specific Unique Unit Code Byte 1

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 1 of Unique Unit Code[1]	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.

2.23.58 F7RC6x - Vendor Specific Unique Unit Code Byte 2

Manufacturing Information Register

Table 91 — F7RC6x: Vendor Specific Unique Unit Code Byte 2

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 2 of Unique Unit Code[1]	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.

2.23.59 F7RC7x - Vendor Specific Unique Unit Code Byte 3

Manufacturing Information Register

Table 92 — F7RC7x: Vendor Specific Unique Unit Code Byte 3

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 3 of Unique Unit Code[1]	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.

2.23.60 F7RC8x - Vendor Specific Unique Unit Code Byte 4

Manufacturing Information Register

Table 93 — F7RC8x: Vendor Specific Unique Unit Code Byte 4

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 4 of Unique Unit Code[1]	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.

2.23.61 F7RC9x - Vendor Specific Unique Unit Code Byte 5

Manufacturing Information Register

Table 94 — F7RC9x: Vendor Specific Unique Unit Code Byte 5

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 5 of Unique Unit Code[1]	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.

2.23.62 F7RCAx - Vendor Specific Unique Unit Code Byte 6

Manufacturing Information Register

Table 95 — F7RCAx: Vendor Specific Unique Unit Code Byte 6

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 6 of Unique Unit Code[1]	Code 0
0	0	0	0	0	0	0	1		Code 1
0	0	0	0	0	0	1	0		Code 2
...									...
1	1	1	1	1	1	0	1		Code 253
1	1	1	1	1	1	1	0		Code 254
1	1	1	1	1	1	1	1		Code 255

1. Programmed and locked in one time programmable memory by DDR4RCD02 vendor.

2.23.63 F7RCBx - Vendor ID Byte 0

Manufacturing Information Register

Table 96 — F7RCBx: Vendor ID Byte 0[1]

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 0 of Vendor ID[2]	VID[7:0] = 0x00h
0	0	0	0	0	0	0	1		VID[7:0] = 0x01h
0	0	0	0	0	0	1	0		VID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		VID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		VID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		VID[7:0] = 0xFFh

1. This is a fixed vendor specific register.
2. As defined for I^2C Function 0 Address 0x00.

2.23.64 F7RCCx - Vendor ID Byte 1

Manufacturing Information Register

Table 97 — F7RCCx: Vendor ID Byte 1[1]

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 1 of Vendor ID[2]	VID[15:8] = 0x00h
0	0	0	0	0	0	0	1		VID[15:8] = 0x01h
0	0	0	0	0	0	1	0		VID[15:8] = 0x02h
...									...
1	1	1	1	1	1	0	1		VID[15:8] = 0xFDh
1	1	1	1	1	1	1	0		VID[15:8] = 0xFEh
1	1	1	1	1	1	1	1		VID[15:8] = 0xFFh

1. This is a fixed vendor specific register.
2. As defined for I^2C Function 0 Address 0x01.

2.23.65 F7RCDx - Device ID Byte 0

Manufacturing Information Register

Table 98 — F7RCDx: Device ID Byte 0[1]

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 0 of Device ID[2]	DID[7:0] = 0x00h
0	0	0	0	0	0	0	1		DID[7:0] = 0x01h
0	0	0	0	0	0	1	0		DID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		DID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		DID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		DID[7:0] = 0xFFh

1. This is a fixed vendor specific register.
2. As defined for I^2C Function 0 Address 0x02.

2.23.66 F7RCEx - Device ID Byte 1

Manufacturing Information Register

Table 99 — F7RCEx: Device ID Byte 1[1]

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Byte 1 of Device ID[2]	DID[15:8] = 0x00h
0	0	0	0	0	0	0	1		DID[15:8] = 0x01h
0	0	0	0	0	0	1	0		DID[15:8] = 0x02h
...									...
1	1	1	1	1	1	0	1		DID[15:8] = 0xFDh
1	1	1	1	1	1	1	0		DID[15:8] = 0xFEh
1	1	1	1	1	1	1	1		DID[15:8] = 0xFFh

1. This is a fixed vendor specific register.
2. As defined for I^2C Function 0 Address 0x03.

2.23.67 F7RCFx - Revision ID

Manufacturing Information Register

Table 100 — F7RCFx: Revision ID[1]

Setting (DA[7:0])								Definition	Encoding
0	0	0	0	0	0	0	0	Revision ID[2]	RID[7:0] = 0x00h
0	0	0	0	0	0	0	1		RID[7:0] = 0x01h
0	0	0	0	0	0	1	0		RID[7:0] = 0x02h
...									...
1	1	1	1	1	1	0	1		RID[7:0] = 0xFDh
1	1	1	1	1	1	1	0		RID[7:0] = 0xFEh
1	1	1	1	1	1	1	1		RID[7:0] = 0xFFh

1. This is a fixed vendor specific register.
2. As defined for I^2C Function 0 Address 0x04.

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3 I²C Bus Interface

For all configuration registers, the DDR4 register supports register access mechanisms through I²C Bus as well as through in-band channel commands. The registers may be read by software from the I²C Bus host at any time the DDR4 register is powered on, except in the DDR4 register clock stopped power down mode or when the device DRST_n pin is asserted.

The DDR4 register I²C Bus interface shall not initiate clock stretching.

The DDR4 register I²C Bus interface must co-exist with an external Temperature Sensor/SPD device on an RDIMM or LRDIMM and shall not inhibit the operation of the I²C Bus when it has no V_{DD} but V_{DDSPD}, even when it goes in and out of clock stopped power down mode.

DDR4 registers are required to support read and write transactions without requiring clock stretching in order to simplify host controller requirements. For similar reasons, DDR4 registers shall not master I²C Bus transactions in normal operation.

3.1 Operating Range

The DDR4 register I²C Bus interface is designed to operate at a voltage range of 2.2-2.8 V and shall operate the I²C Bus up to 1 MHz maximum (Fast Mode+).

3.2 External Pins

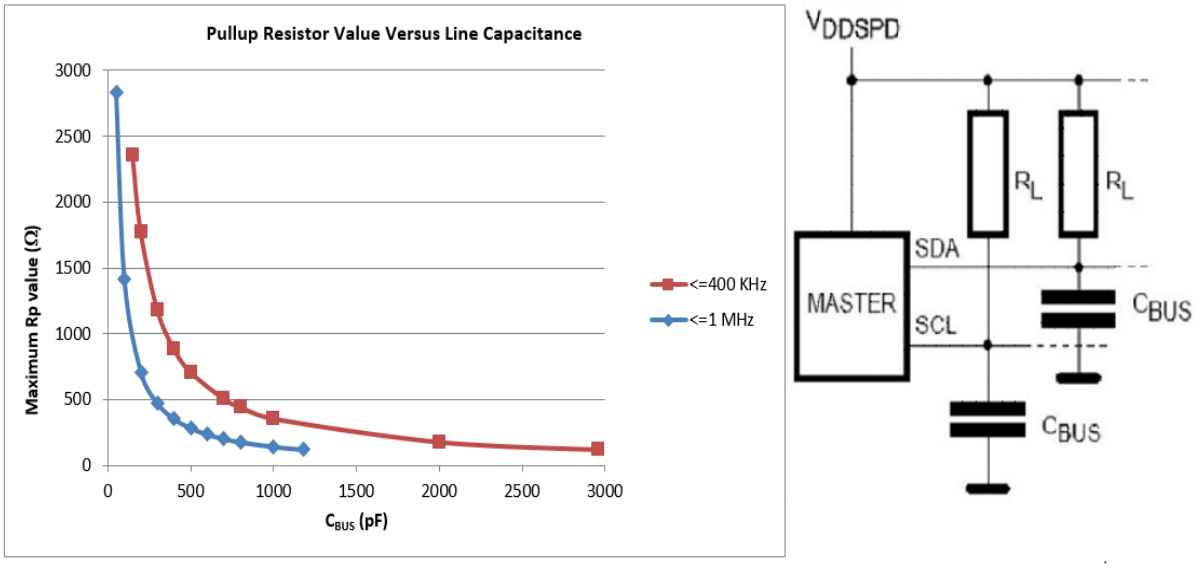
The DDR4 register I²C Bus interfaces uses the following five external device pins.

3.2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{DDSPD}. (Figure 31 on page 108 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

3.2.2 Serial Data (SDA)

This bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to the most positive V_{DDSPD} in the I²C Bus chain. Figure 31 on page 108 indicates how the value of the pull-up resistor can be calculated.



Formula (KΩ): $$Rp(max) = \frac{tr}{0.847\ x\ C_{Bus}}$$

$$Rp(min) = \frac{VDDSPD(max) - VOL(max)}{IOL(min)} \qquad Rp(min) = (2.8V - 0.4V)/20mA \qquad Rp(min) = 120\ \Omega$$

Figure 31 — Maximum R_L Value Versus Bus Capacitance (C_{BUS}) for an I^2C Bus

3.2.3 Select Address (SA0, SA1, SA2)

These input signals are used to set the value of the three least significant bits of the 7-bit Slave Address. In the Dual Inline Memory Module (DIMM) application, the Select Address inputs SA[2:1] of the DDR4 register must be connected to V_{SS} or V_{DDSPD} directly (that is without using a pull-up or pull-down resistor) through the DIMM socket (see Table 101 on page 108). SA0 is connected to the DIMM gold finger through a 1 KΩ series resistor used during high voltage programming of the SPD device on the DIMM. The pull-up resistors needed for correct operation of the I^2C Bus are located on the motherboard. The device shall interpret V_{DDSPD} on the SA[2:0] pins as a logic '1' and V_{SS} as a logic '0'.

Table 101 — Unique I^2C Bus Addressing of DDR4 Registers in DIMM Applications

Slave address [2:0]	SA2	SA1	SA0
000	0	0	0
001	0	0	1
010	0	1	0
011	0	1	1
100	1	0	0

Table 101 — Unique I²C Bus Addressing of DDR4 Registers in DIMM Applications

Slave address [2:0]	SA2	SA1	SA0
101	1	0	1
110	1	1	0
111	1	1	1
Note 1: 0 = V_{SS}, 1 = V_{DDSPD}			

The address bits (SA0-SA2) of the DDR4RCD02 are connected to corresponding address pins (SA0-SA2) of the SPD/TSOD device on the DIMM - see Figure 32 on page 109.

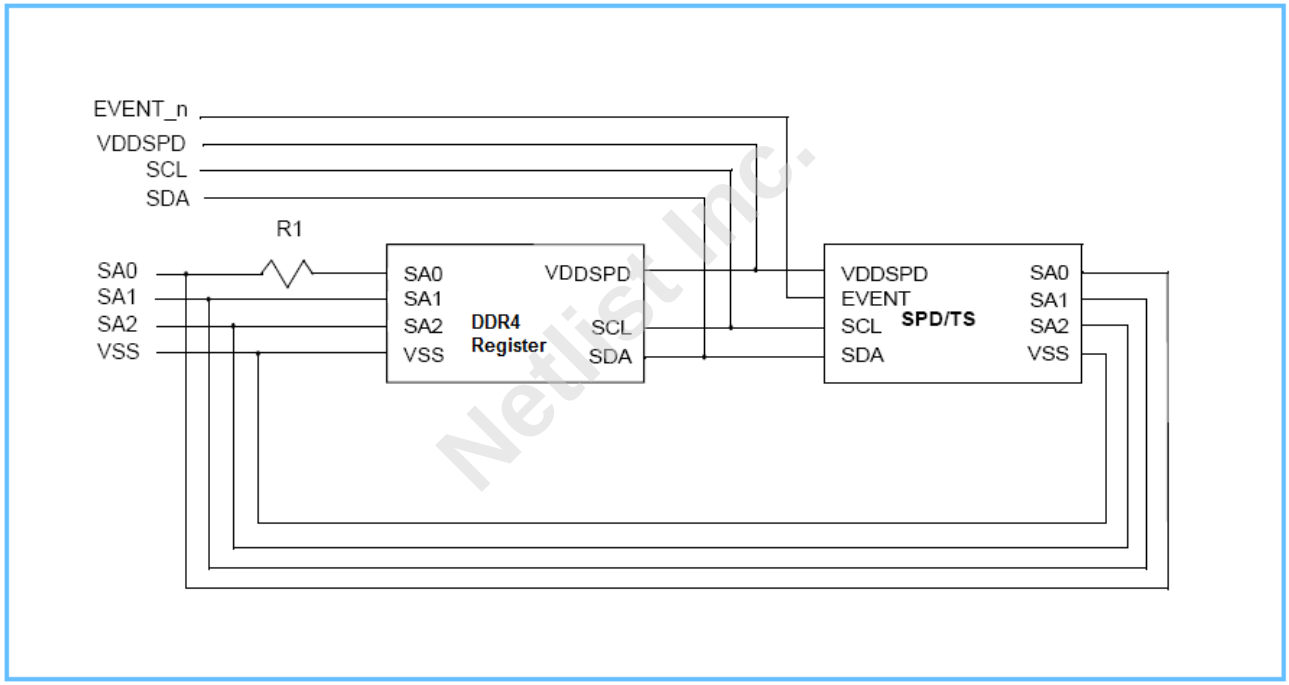


Figure 32 — I²C Bus Wiring Diagram

3.3 System Management Access

System Management software in the platform can initiate system management access to the configuration registers. This can be done through I²C Bus accesses.

DDR4RCD02 components contain an I²C Bus slave port and allow access to the configuration registers.

I²C Bus operations are made up of two major steps: (1) writing information to registers within each component and (2) reading configuration registers from each component. The following sections will describe the protocol for an I²C Bus master to access an DDR4 register component's internal configuration registers.

3.3.1 Slave Address

The 7-bit slave address used for each primitive I^2C Bus transaction is determined by the SA[2:0] pins and the 4-bit device address.

- Primary I^2C Bus address (BFUNC pin strapped to V_{SS}):
  - — Slave Address[6:3] = 4'b1011
  - — Slave Address[2:0] = SA[2:0][1]
- Secondary I^2C Bus address (e.g. for a secondary register; BFUNC pin strapped to V_{DD}):
  - — Slave Address[6:3] = 4'b1000
  - — Slave Address[2:0] = SA[2:0][1]

3.3.2 Supported I^2C Bus Commands

The DDR4 register component's I^2C slave port supports register reads and writes built out of the following four I^2C Bus primitive commands:

Block Write **Byte Write**

Block Read **Byte Read**

The DDR4 register is not required to support block accesses larger than a double word.

Each I^2C Bus transaction has an 8-bit command driven by the master. The format for this command is illustrated in . Table 102, "I2C Bus command Encoding" below.

Table 102 — I^2C Bus command Encoding

7	6	5	4	3:2	1:0
Begin	End	Rsvd	PEC_en	Internal Command: **00 - Read DWord** **01 - Write Byte** **10 - Write Word** **11 - Write DWord**	I^2C Bus Command: **00 - Byte** 01 - *Rsvd* **10 - Block** 11 - *Rsvd*

The *Begin* bit indicates the first transaction of a read or write sequence.

The *End* bit indicates the last transaction of a read or write sequence.

The *PEC_en* bit enables the 8-bit PEC generation and checking logic.

The *Internal Command* field specifies the internal command to be issued by the I^2C Bus slave logic. Note that the Internal Command must remain consistent (i.e. not change) during a sequence that accesses a configuration register. Operation cannot be guaranteed if it is not consistent when the command setup sequence is done.

The *I^2C Bus Command* field specifies the I^2C Bus command to be issued on the bus. This field is used as an indication of the length of transfer so the slave knows when to expect the PEC packet (if enabled).

Reserved bits should be written to zero to preserve future compatibility.

Hosts are required to form commands that are internally self consistent. The length indicated by the internal command should be consistent with the byte count and the DDR4 register behavior will be undefined when the internal command is inconsistent with the bye count.

1. See Table 101 for details

3.3.3 Register Access Protocols

Sequences of these basic commands will initiate internal accesses to the component's configuration registers.

Each configuration read or write first consists of an I^2C Bus write sequence which initializes the register's address . The term sequence is used since these variables may be written with a single block write or multiple byte writes. Once these parameters are initialized, the I^2C Bus master can initiate a read sequence (which performs a configuration read) or a write sequence (which performs a configuration write).

Note that all register control words are located in the I^2C Bus Function 0 - 7 address spaces. This leaves the address space of the other seven I^2C Bus functions available for vendor specific test and debug registers which are not defined in this specification.

Table 103 — I^2C Bus Protocol Addressing fields

Address Field Name	Bits	Description
Reserved	7:0	Reserved - Device may alias all these addresses to 00h
Dev	3:0	Reserved - Device may alias all these addresses to 00h
Function	3:0	Function Address
Reg_Num[15:8]	7:0	Reserved - Device may alias all these addresses to 00h
Reg_Num[7:0]	7:0	Register Address within Function

3.3.3.1 Access Mechanism

For all configuration & status registers, the DDR4RCD02 supports register access mechanisms through I^2C Bus as well as through in-band channel commands. The registers may be read by software from the I^2C Bus host at any time the DDR4RCD02 is powered on, except in the register clock stopped power down mode or when the device DRST_n pin is asserted.

Table 104 shows the mapping between DDR4RCD02 control words and I^2C Bus register numbers. The entire register space of the DDR4RCD02 is accessible with the I^2C Bus Reg_Num[7:0] address field.

Table 104 — Function 0 I^2C Bus Address Map

Register Address	Description	D7	D6	D5	D4	D3	D2	D1	D0	CW access
0x00h	Vendor ID	VID[7:0]								No
0x01h		VID[15:8]								No
0x02h	Device ID	DID[7:0]								No
0x03h		DID[15:8]								No
0x04h	Revision ID	RID[7:0]								No
0x05h	Reserved									No
0x06h	Reserved	Reserved								No
0x07h	Reserved									No
0x08h	4-bit RCWs	F0RC01				F0RC00				Yes
0x09h	4-bit RCWs	F0RC03				F0RC02				Yes
0x0Ah	4-bit RCWs	F0RC05				F0RC04				Yes
0x0Bh	4-bit RCWs	F0RC07				F0RC06				Yes
0x0Ch	4-bit RCWs	F0RC09				F0RC08				Yes
0x0Dh	4-bit RCWs	F0RC0B				F0RC0A				Yes
0x0Eh	4-bit RCWs	F0RC0D				F0RC0C				Yes
0x0Fh	4-bit RCWs	F0RC0F				F0RC0E				Yes
0x10h	8-bit RCW	F0RC1x								Yes
0x11h	8-bit RCW	F0RC2x								Yes
0x12h	8-bit RCW	F0RC3x								Yes
0x13h	8-bit RCW	F0RC4x								Yes
0x14h	8-bit RCW	F0RC5x								Yes
0x15h	8-bit RCW	F0RC6x								Yes
0x16h	8-bit RCW	F0RC7x								Yes
0x17h	8-bit RCW	F0RC8x								Yes
0x18h	8-bit RCW	F0RC9x								Yes
0x19h	8-bit RCW	F0RCAx								Yes
0x1Ah	8-bit RCW	F0RCBx								Yes
0x1Bh	8-bit RCW	F0RCCx								Yes
0x1Ch	8-bit RCW	F0RCDx								Yes
0x1Dh	8-bit RCW	F0RCEx								Yes
0x1Eh	8-bit RCW	F0RCFx								Yes

Note: CWs residing in FN[15:1] will start at register address 0x08

The DDR4RCD02 Device ID is DID = 0x0042.

"Reserved" means that this register space is reserved for future extensions (that are common to all implementations).

"Vendor specific" means that this register space is available now for vendor specific test and debug registers.

Each byte of the DDR4RCD02 register space has its own unique address. For CSR writes the RCD registers can be accessed in byte (8-bit), word (16-bit) or double word (32-bit) quantities. For CSR reads the device registers can only be accessed in double word (32-bit) quantities.

All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). As an example Table 105 defines the byte order for double word accesses to the DDR4RCD02 control words.

In this chapter CSRs are defined as 8-bit registers. Since a byte is the smallest access granularity for CSRs, a single 8-bit CSR contains two 4-bit control words.

Table 105 — Double word byte order for I^2C Bus control word accesses

Description	Data[31:24]		Data[23:16]		Data[15:8]		Data[7:0]	
F0RC00-F0RC07	F0RC07[3:0]	F0RC06[3:0]	F0RC05[3:0]	F0RC04[3:0]	F0RC03[3:0]	F0RC02[3:0]	F0RC01[3:0]	F0RC00[3:0]
F0RC08-F0RC0F	F0RC0F[3:0]	F0RC0E[3:0]	F0RC0D[3:0]	F0RC0C[3:0]	F0RC0B[3:0]	F0RC0A[3:0]	F0RC09[3:0]	F0RC08[3:0]
F0RC1x-F0RC4x	F0RC4x[7:0]		F0RC3x[7:0]		F0RC2x[7:0]		F0RC1x[7:0]	
F0RC5x-F0RC8x	F0RC8x[7:0]		F0RC7x[7:0]		F0RC6x[7:0]		F0RC5x[7:0]	
F0RC9x-F0RCCx	F0RCCx[7:0]		F0RCBx[7:0]		F0RCAx[7:0]		F0RC9x[7:0]	
F0RCDx-F0RCFx			F0RCFx[7:0]		F0RCEx[7:0]		F0RCDx[7:0]	

3.3.3.2 Configuration Register Read Protocol

Configuration reads are accomplished through an I^2C Bus write(s) and later followed by an I^2C Bus read. The write sequence is used to initialize the Bus Number, Device, Function, and Register Number for the configuration access.

The writing of this information can be accomplished through any combination of the supported I^2C Bus write commands (Block, Byte). The *Internal Command* field for each write should specify Read DWord.

All I^2C Bus configuration reads should be DWord aligned. The DDR4 register will ignore the lowest two bits of the register address and return the four bytes within a DWord in the byte order shown in the following examples, i.e. most significant byte (Data[31:24]) first and least significant byte (Data[7:0]) last.

After all the information is set up, the last write (*End* bit is set) initiates an internal configuration read. If an error occurs during the internal access, the last write command will receive a NACK. A status field indicates abnormal termination and contains status information such as target abort, master abort, and time-outs. The status field encoding is defined in the following table.

Table 106 — Status Field Encoding for I^2C Bus Reads

Bit	Description
7	Reserved
6	Reserved
5	Reserved

Table 106 — Status Field Encoding for I²C Bus Reads

Bit	Description
4	Internal Target Abort
3:1	Reserved
0	Successful

Examples of configuration reads are illustrated below. All of these examples have PEC (Packet Error Code) enabled. If the master does not support PEC, then bit 4 of the command would be cleared and there would not be a PEC phase. For I²C Bus read transactions, the last byte of data (or the PEC byte if enabled) is NACKed by the master to indicate the end of the transaction. For diagram compactness, "Register Number[]" is also sometimes referred to as "Reg Number" or "Reg Num".

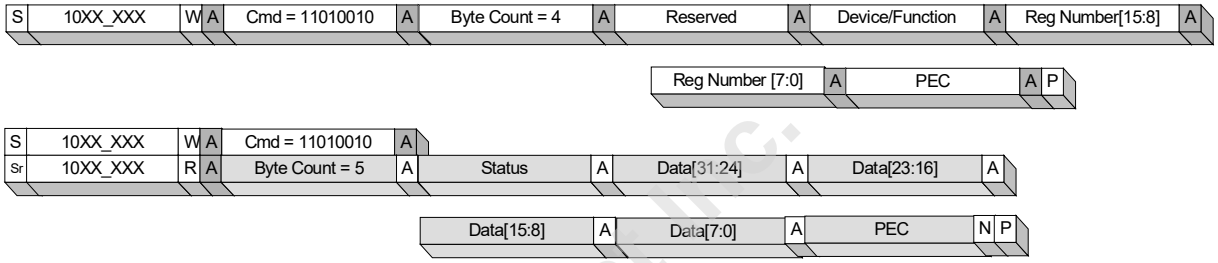


Figure 33 — I²C Bus Configuration Read (Block Write / Block Read, PEC enabled)

The following example uses byte writes and reads.

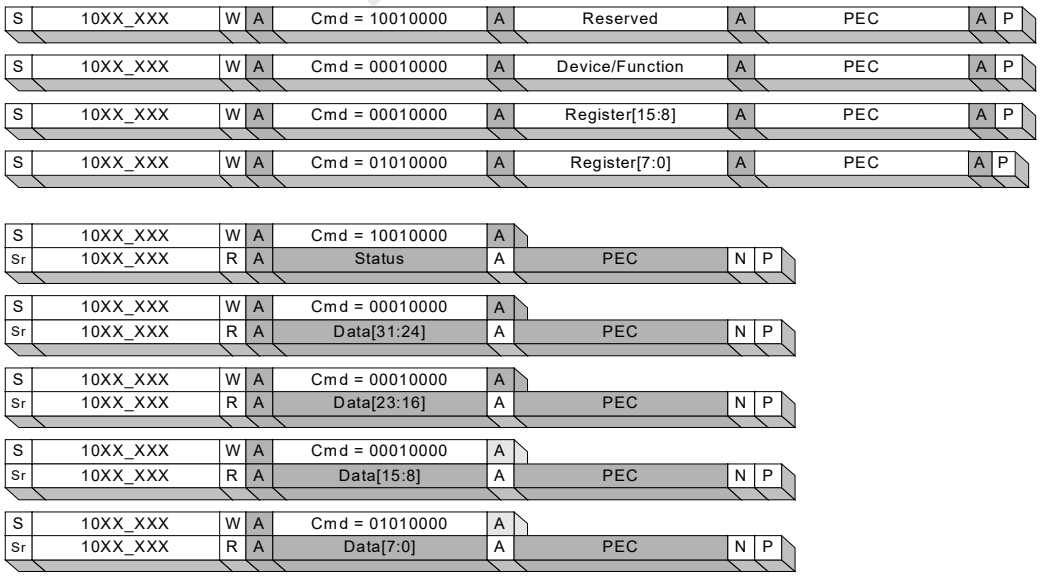


Figure 34 — I²C Bus Configuration Read (Write Bytes / Read Bytes, PEC enabled)

3.3.3.3 Configuration Register Write Protocol

Configuration writes are accomplished through a series of I^2C Bus writes. As with configuration reads, a write sequence is first used to initialize the Bus Number, Device, Function, and Register Number for the configuration access. The writing of this information can be accomplished through any combination of the supported I^2C Bus write commands (Block, Byte).

On I^2C Bus, there is no concept of byte enables. Therefore, the Register Number written to the slave is assumed to be aligned to the length of the Internal Command. In other words, for a Write Byte internal command, the Register Number specifies the byte address. For a Write DWord internal command, the two least-significant bits of the Register Number are ignored. This is different from PCI where the byte enables are used to indicate the byte of interest.

After all the information is set up, the I^2C Bus master initiates one or more writes which sets up the data to be written. The final write (*End* bit is set) initiates an internal configuration write. If an error occurred, the I^2C Bus interface NACKs the last write operation just before the stop bit.

Examples of configuration writes are illustrated below.

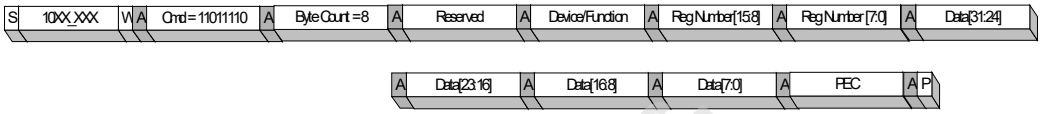


Figure 35 — I^2C Bus Configuration Double Word Write (Block Write, PEC enabled)

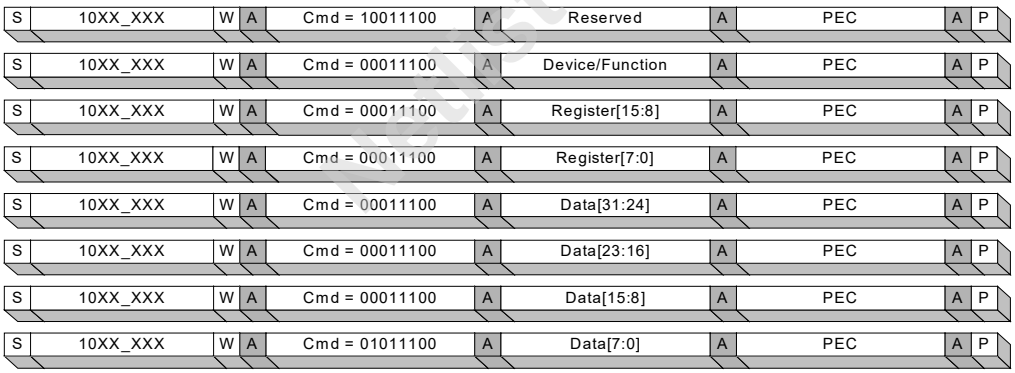


Figure 36 — I^2C Bus Configuration Double Word Write (Write Bytes, PEC enabled)

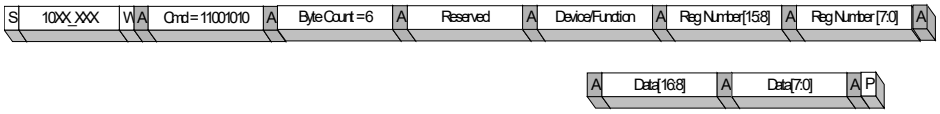


Figure 37 — I^2C Bus Configuration Word Write (Block Write, PEC disabled)

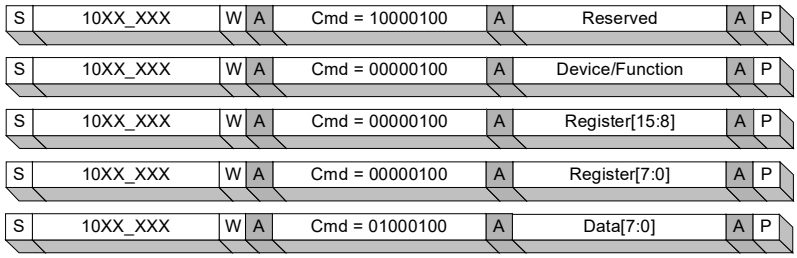


Figure 38 — I²C Bus Configuration Byte Write (Write Bytes, PEC disabled)

3.4 I²C Bus Error Handling

The I²C Bus slave interface handles two types of errors: internal and PEC. These errors manifest as a Not-Acknowledge (NACK) for the read command (*End* bit is set). If an internal error occurs during a configuration write, the final write command receives a NACK just before the stop bit. If the master receives a NACK, the entire configuration transaction should be reattempted.

If the master supports packet error checking (PEC) and the PEC_en bit in the command is set, then the PEC byte is checked in the slave interface. If the check indicates a failure, then the slave will NACK the PEC packet.

3.5 I²C Resets

3.5.1 I²C Interface State Machine Reset

The slave interface state machine can be reset by the master in two ways :

- The master holds SCL low for 35 ms cumulative. Cumulative in this case means that all the “low time” for SCL is counted between the Start and Stop bit. If this totals 35 ms before reaching the Stop bit, the interface is reset.
  - Timing is set up to be 35 ms for 1600 MT/s and may scale down at higher frequencies
    * 30 ms at 1866 MT/s
    * 26.25 ms at 2133 MT/s
    * 23.33 ms at 2400 MT/s
    * 21 ms at 2666 MT/s
    * 19.09 ms at 2933 MT/s
    * 17.5 ms at 3200 MT/s
- The master holds SCL continuously high for 100 µs between Start and Stop conditions.
  - Timing is set up to be 100 µs for 1600 MT/s and may scale down at higher frequencies
    * 85 µs at 1866 MT/s
    * 75 µs at 2133 MT/s
    * 66.67 µs at 2400 MT/s
    * 60 µs at 2666 MT/s
    * 54.10 µs at 2933 MT/s
    * 50 µs at 3200 MT/s

3.5.2 I²C transactions during reset

Since the configuration registers are affected by the DRST_n pin, I^2C masters will NOT be able to access the device registers while the device is reset.

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4 Absolute maximum ratings

Table 107 — Absolute maximum ratings over operating free-air temperature range [1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	Supply voltage		– 0.3	1.5	V
V_{IN}	Receiver input voltage[2]	See Note 4 and 5	– 0.3	V_{DD} + 0.5	V
V_{REF}	Reference voltage		– 0.3	V_{DD} + 0.5	V
V_{OUT}	Driver output voltage[3]	See Note 4 and 6	– 0.3	V_{DD} + 0.5	V
I_{IK}	Input clamp current	$V_{IN} < 0$ or $V_{IN} > V_{DD}$	-	-50	mA
I_{OK}	Output clamp current	$V_{OUT} < 0$ or $V_{OUT} > V_{DD}$	-	± 50	mA
I_{OUT}	Continuous output current	$0 < V_{OUT} < V_{DD}$	-	± 50	mA
I_{CCC}	Continuous current through each V_{DD} or V_{ss} pin		-	± 100	mA
T_{stg}	Storage temperature		– 65	+ 150	°C

NOTE 1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: This parameter does not apply to SA[2:0] and SCL. See I^2C chapter for voltage specifications for these inputs.

NOTE 3: This parameter does not apply to SDA. See I^2C chapter for voltage specifications for this output.

NOTE 4: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

NOTE 5: This value is limited to 1.50 V maximum.

5 Input AC and DC Specifications

The DDR4RCD02 parametric values are specified for the device default control word settings, unless otherwise stated. The device must meet the electrical and timing characteristics with any programmed drive strength setting. Note that the F0RC0A setting does not affect any of the parametric values. .

Table 108 — Operating Electrical Characteristics

Symbol	Parameter	Applicable Signals	Condition	Min	Nom	Max	Unit
V_{DD}, PV_{DD}	DC Supply voltage[1]		1.2 V Operation	1.14	1.2	1.26	V
AV_{DD}	DC Supply voltage before filter[2]		1.2 V Operation	1.13	1.2	1.26	V
V_{TT}	DC Termination voltage[3]			$V_{DDnom}/2$ -45	$V_{DDnom}/2$	$V_{DDnom}/2$+45	mV
V_{REF}	DC Reference voltage[1,4]	VrefCA		0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	mV
$V_{IH.CMOS}$	HIGH-level input voltage	DRST_n		see Table 116			V
$V_{IL.CMOS}$	LOW-level input voltage						V
$V_{IH.ERROR}$	HGH-level input voltage	ERROR_IN_n		0.75 x V_{DD} + 80			mV
$V_{IL.ERROR}$	LOW-level input voltage					0.75 x V_{DD} - 80	mV
$V_{IL(static)}$	LOW-level input voltage	CK_t/CK_c during clock stop		0	-	0.35 x V_{DD}	mV
V_{IX}(CK)	Differential input cross point voltage range[5]	CK_t/CK_c		see Table 113			mV
V_{IX_EX}(CK)	Extended differential input cross point voltage range						mV
$V_{CM(DC)}$	Average common mode DC voltage			0.46 x V_{DD}	0.5 x V_{DD}	0.54 x V_{DD}	mV
V_{SEH}	Single-ended high level			see Table 112			mV
V_{SEL}	Single-ended low level						mV
$V_{IH(AC)}$	AC input high level			see Table 110, “AC and DC Input Levels for CK,”			V
$V_{IL(AC)}$	AC input low level						V
V_{IHdiff}	Differential input high level						V
V_{ILdiff}	Differential input low level						V
$V_{IHdiff(AC)}$	AC differential input high level						V
$V_{ILdiff(AC)}$	AC differential input low level						V
$V_{OH(AC)}$	AC output high level	All outputs except ALERT_n		V_{TT} + 0.15 x V_{DD}	-	-	V
$V_{OL(AC)}$	AC output low level			-	-	V_{TT} - 0.15 x V_{DD}	V
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	Yn_t/Yn_c, BCK_t/BCK_c		-	+ 0.3 * V_{DD}	-	V
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)			-	- 0.3 * V_{DD}	-	V
$V_{OD\_clock(AC)}$	Differential re-driven clock swing	Yn_t/Yn_c, BCK_t/BCK_c		(1/3) x V_{DD}		V_{DD}	V
V_{OX}(clock)	Differential output cross point voltage			see Table 125			mV
T_j	Junction temperature[6]			0	-	125	°C
T_{case}	Case temperature		Measurement procedure JESD51-2	-	-	103[7]	°C
T_{j_ext}	Extended junction temperature[8,9]			-40	-	125	°C
T_{case_ext}	Extended case temperature[8]		Measurement procedure JESD51-2	-40	-	103[10]	°C

1. DC bandwidth limited to 20 MHz.
2. See filter schematics and dimensioning in Figure 80 on page 172.
3. If V_{TT} is out of the range, QCA output drive strength will not be guaranteed.
4. Only valid when F0RC0B DA3 = 1.
5. See Diagram (Figure 71)
6. For operation beyond Tj min and max datasheet values are not guaranteed and may de-rate. For operation above Tj max lifetime could be affected. All parametric measurements are performed at 0 °C, 25 °C and 95 °C.
7. This spec is meant to guarantee a Tj of 125 °C by the DDR4RCD02. Since Tj cannot be measured or observed by users, Tcase is specified instead. Under all thermal condition, the Tj of a DDR4RCD02 shall not be higher than 125 °C.
8. Extended temperature range support is an optional feature. Devices supporting this feature are identified by appending "X" to the device name. For example, DDR4RCD02X and DDR4RCD02NVX support extended temperature range while DDR4RCD02 and DDR4RCD02NV do not support extended temperature range.
9. For operation beyond Tj_ext min and max datasheet values are not guaranteed and may de-rate. For operation above Tj_ext max lifetime could be affected. All parametric measurements are performed at -40 °C, 25 °C and 95 °C.
10. This spec is meant to guarantee a Tj_ext of 125 °C by the DDR4RCD02. Since Tj_ext cannot be measured or observed by users, Tcase_ext is specified instead. Under all thermal condition, the Tj_ext of a DDR4RCD02 shall not be higher than 125 °C.

5.1 CA Input Receiver Specifications

The CA input receiver mask for voltage and timing is shown in Figure 39. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DDR4RCD02 input receiver to successfully capture a valid input signal with BER < 1e-18. The mask is a receiver property for each pin and it is not the valid data eye.

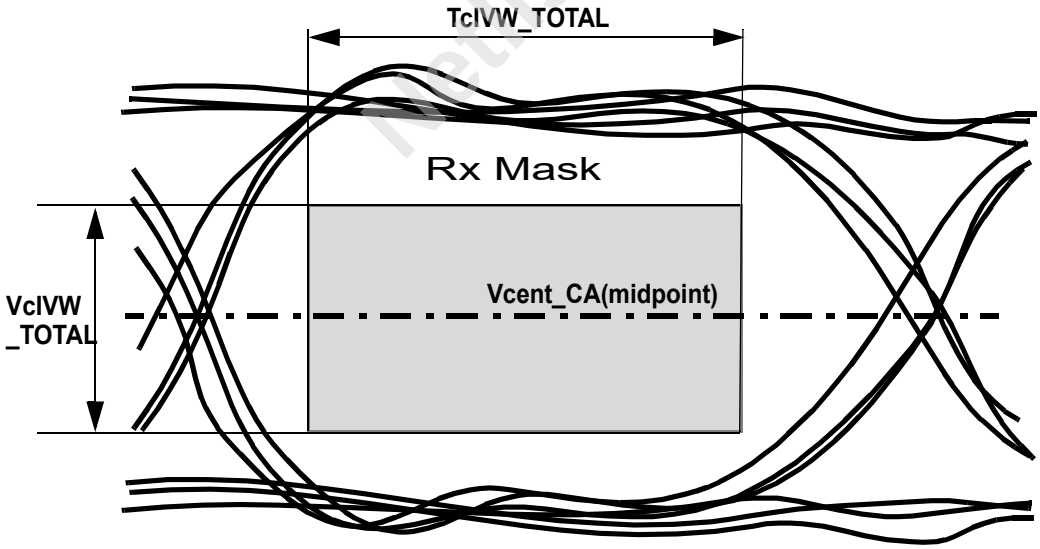


Figure 39 — CA Receiver(Rx) mask

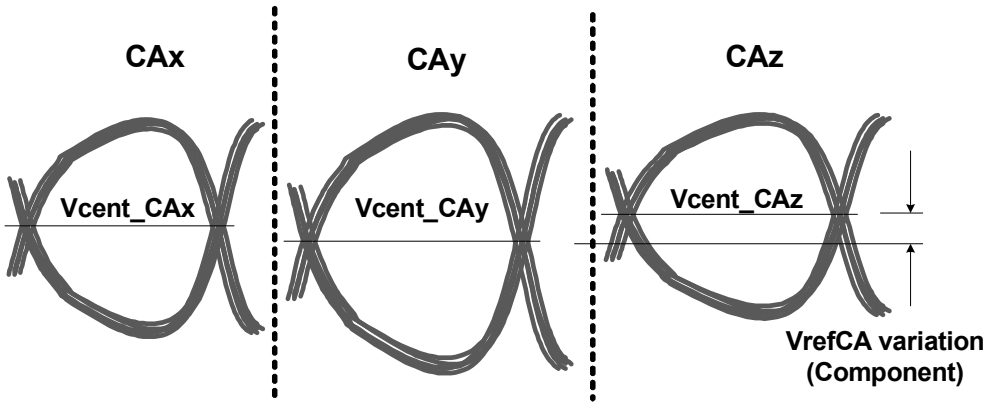
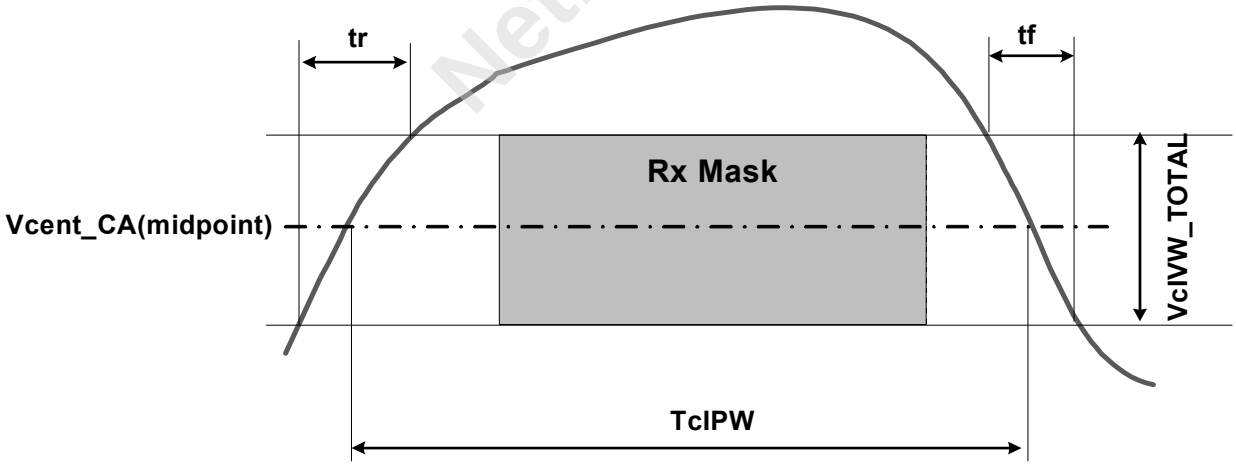


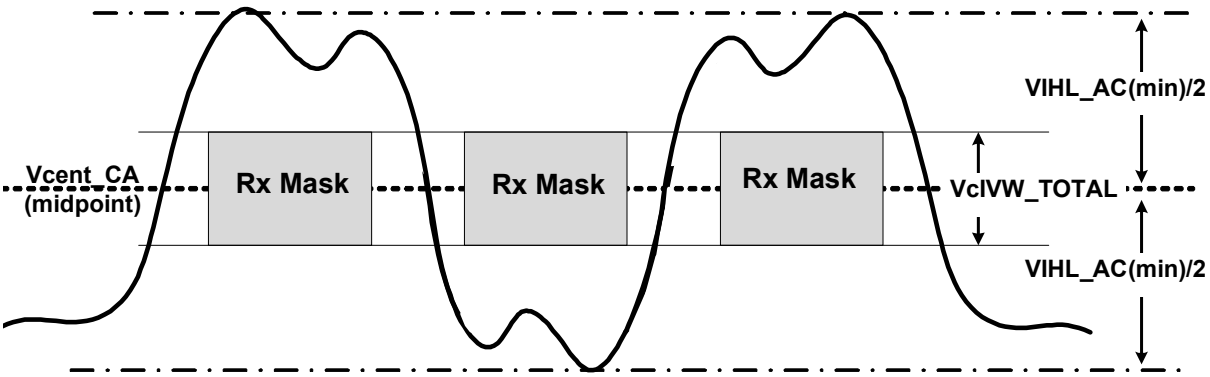
Figure 40 — Across pin Vcent_CA voltage variation

Vcent_CA(midpoint) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all ADD/CMD and CTRL (=CA) pins for a given DDR4RCD02 component. Each CA pin Vcent level is defined by the center, i.e. widest opening of the cumulative data input eye as depicted in Figure 40. This clarifies that any DDR4RCD02 component level variation must be accounted for within the DDR4RCD02 Rx mask. The VrefCA will be set by the system to account for Ron and IBT settings.



NOTE 1: SRIN_cIVW=VcIVW_TOTAL/(tr or tf)

Figure 41 — CA TcIPW and SRIN_clVW definition (for each input pulse)



NOTE 1: The VIHL_AC(min) requirement has to be met for any UI making a transition. It does not have to be met for a UI when there is no signal transitions.

Figure 42 — VIHL_AC(min) requirement (for each input pulse)

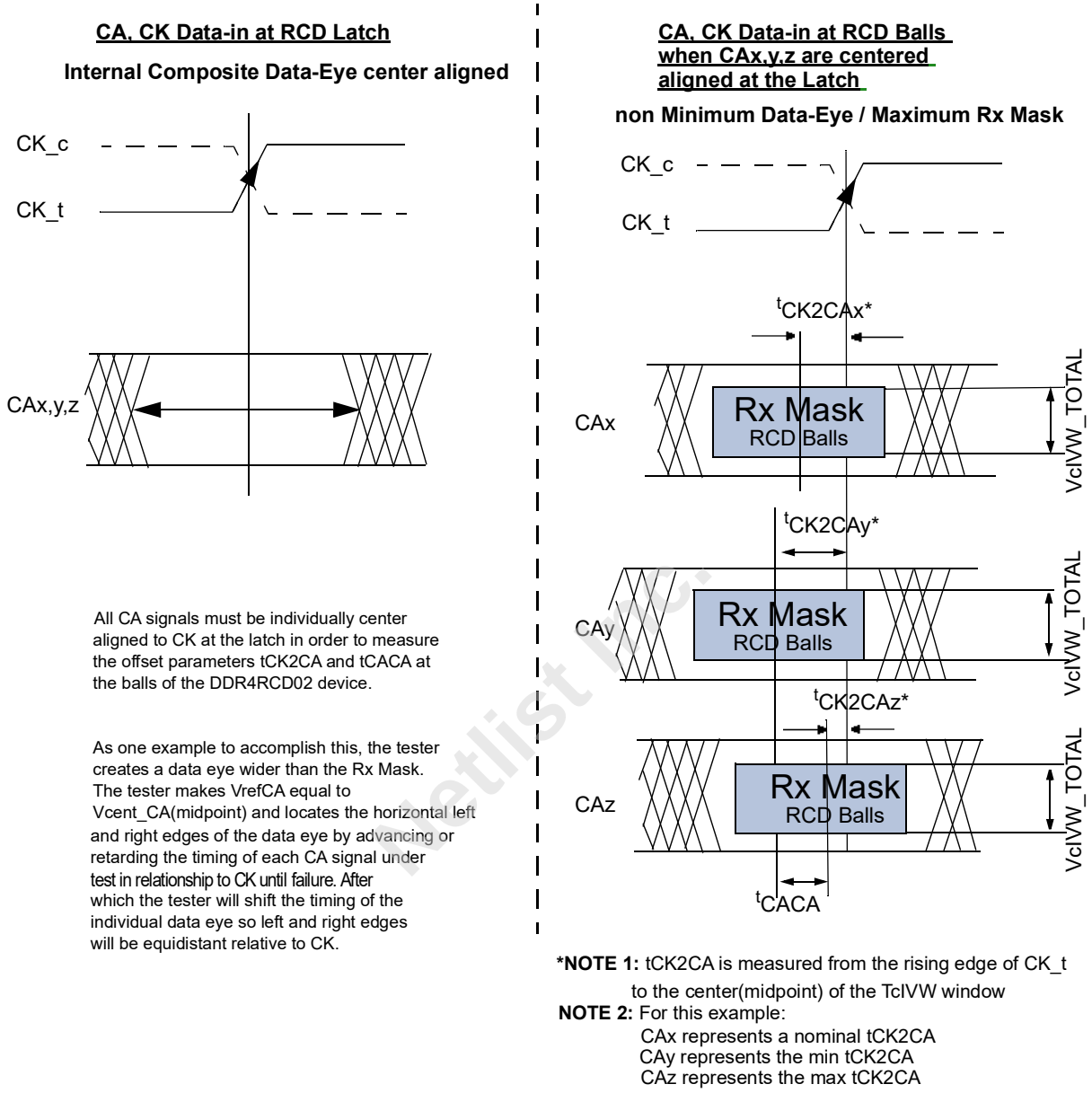


Figure 43 — CK to CA Timings at the DDR4RCD02 balls referenced from the internal latch

All of the timing terms in Figure 43 are measured from CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_TOTAL voltage levels centered around Vcent_CA(midpoint). In Figure 43 the timings at the balls are referenced with respect to all CA signals center aligned to the DDR4RCD02 internal latch. The data to data offset tCACA is defined as the magnitude of the difference between the min and max tCK2CA for a given component.

Table 109 — CA Input Receiver Voltage Margin and AC Timing by Speed Bin for DDR4-1600 -3200

Speed		DDR4-1600/ 1866/2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	NOTE
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VcIVW_TOTAL	Rx Mask p-p voltage total	-	150	-	120	-	120	-	110	-	100	mV	1,2,3,4
TcIVW_TOTAL	Rx timing window total	-	0.2	-	0.15	-	0.15	-	0.135	-	0.135	UI	1,4
VIHL_AC	CA AC input pulse amplitude pk-pk	180	-	150	-	140	-	130	-	120	-	mV	5
TcIPW	CA input pulse width	0.5	-	0.4	-	0.3	-	0.3	-	0.3	-	UI	6
tCK2CA	CK to CA offset	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	UI	7
tCACA	CA to CA offset	-	0.04	-	0.04	-	0.04	-	0.04	-	0.04	UI	8
SRIN_cIVW	Input Slew Rate over VcIVW_TOTAL	1	5	1	5	1	5	1	5	1	5	V/ns	9

* UI=tck(avg)min

NOTE 1: CA Rx mask voltage and timing total input valid window where VcIVW is centered around Vcent_CA(midpoint). The data Rx mask is applied per bit and includes voltage and temperature drift terms. The design specification is BER ≤1e-18.
NOTE 2: Rx mask voltage AC swing peak-peak requirement over TcIVW_TOTAL with at least half of VcIVW_TOTAL(max) above Vcent_CA(midpoint) and at least half of VcIVW_TOTAL(max) below Vcent_CA(midpoint).
NOTE 3: The VcIVW voltage levels are centered around Vcent_CA(midpoint).
NOTE 4: Overshoot and Undershoot Specifications see Table 117 and Figure 50.
NOTE 5: CA input pulse signal swing into the receiver must meet or exceed VIHL_AC for at least one point over the duration of TcIPW for any UI during which there is a signal transition. No timing requirement above level. VIHL_AC is the peak to peak voltage centered around Vcent_CA(midpoint), which is defined in Figure 40.
NOTE 6: CA minimum input pulse width defined at the Vcent_CA(midpoint).
NOTE 7: CK to CA offset defined within all ADD/CMD and CTRL inputs at DDR4RCD02 balls. Includes all DDR4RCD02 process, voltage and temperature variation.
NOTE 8: CA to CA offset is defined as the magnitude of the difference between the min and max CK to CA offset at DDR4RCD02 balls for a given component. Includes all DDR4RCD02 voltage and temperature variation.
NOTE 9: Input slew rate over VcIVW Mask centered at Vcent_CA(midpoint). . This single-ended slew rate also applies to CK_t and CK_c.

5.2 AC and DC Logic Input Levels for Differential Signals

5.2.1 Differential signal definition

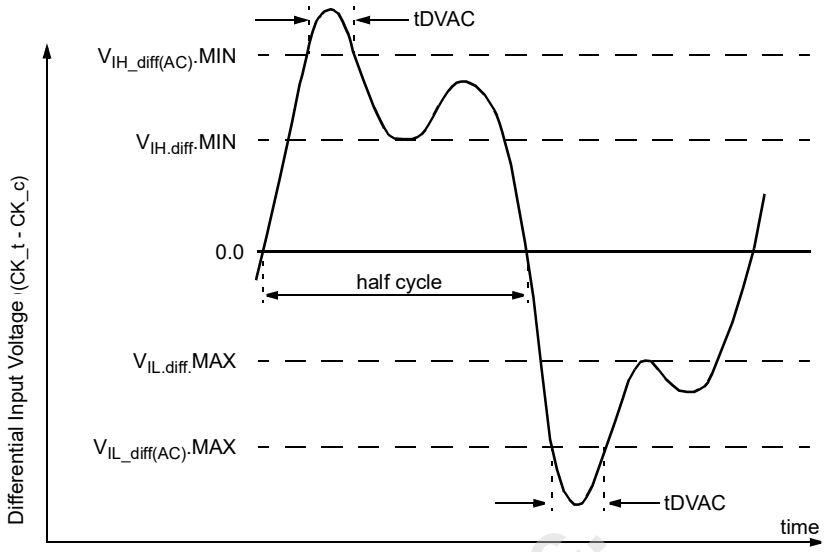


Figure 44 — Definition of differential AC-swing and "time above AC-level" t_{DVAC}

NOTE 1: Differential signal rising edge from $V_{IL.diff}$.MAX to V_{IH_diff}.MIN must be monotonic slope.
NOTE 2: Differential signal falling edge from $V_{IH.diff}$.MIN to V_{IL_diff}.MAX must be monotonic slope.

5.2.2 Differential swing requirements for CK_t/CK_c

Table 110 — AC and DC Input Levels for CK

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		Unit	NOTE
		Min	Max	Min	Max	Min	Max		
$V_{IH(AC)}$	AC input high	$V_{REF}CA$ + 90	Note 4	$V_{REF}CA$ + 75	Note 4	$V_{REF}CA$ + 70	Note 4	mV	1, 2
$V_{IL(AC)}$	AC input low	Note 4	$V_{REF}CA$ - 90	Note 4	$V_{REF}CA$ - 75	Note 4	$V_{REF}CA$ - 70	mV	1, 2
$V_{IH.diff}$	Differential input high	+130	Note 4	+100	Note 4	+90	Note 4	mV	3
$V_{IL.diff}$	Differential input low	Note 4	-130	Note 4	-100	Note 4	-90	mV	3
$V_{IH\_diff(AC)}$	AC differential input high	2 x ($V_{IH(AC)}$.MIN - $V_{REF}CA$)	Note 4	2 x ($V_{IH(AC)}$.MIN - $V_{REF}CA$)	Note 4	2 x ($V_{IH(AC)}$.MIN - $V_{REF}CA$)	Note 4	mV	2
$V_{IL\_diff(AC)}$	AC differential input low	Note 4	2 x ($V_{IL(AC)}$.MAX - $V_{REF}CA$)	Note 4	2 x ($V_{IL(AC)}$.MAX - $V_{REF}CA$)	Note 4	2 x ($V_{IL(AC)}$.MAX - $V_{REF}CA$	mV	2

Symbol	Parameter	DDR4-2933		DDR4-3200		Unit	NOTE
		Min	Max	Min	Max		
$V_{IH(AC)}$	AC input high	$V_{REF}CA$ + 65	Note 4	$V_{REF}CA$ +65	Note 4	mV	1, 2
$V_{IL(AC)}$	AC input low	Note 4	$V_{REF}CA$ - 65	Note 4	$V_{REF}CA$ - 65	mV	1, 2
$V_{IH.diff}$	Differential input high	+80	Note 4	+ 80	Note 4	mV	3
$V_{IL.diff}$	Differential input low	Note 4	- 80	Note 4	- 80	mV	3
$V_{IH\_diff(AC)}$	AC differential input high	2 x ($V_{IH(AC)}$.MIN - $V_{REF}CA$)	Note 4	2 x ($V_{IH(AC)}$.MIN - $V_{REF}CA$)	Note 4	mV	2
$V_{IL\_diff(AC)}$	AC differential input low	Note 4	2 x ($V_{IL(AC)}$.MAX - $V_{REF}CA$)	Note 4	2 x ($V_{IL(AC)}$.MAX - $V_{REF}CA$)	mV	2

NOTE 1: This is a single-ended parameter. It is used to define the differential input specs.
NOTE 2: $V_{REF}CA$ is either the voltage from the external VrefCA input pin or the output of the internal $V_{REF}CA$ generator
NOTE 3: Used to define a differential signal slew-rate.
NOTE 4: These values are not defined, however the differential signals CK_t, CK_c need to meet the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications”

Table 111 — Allowed time before ringback (tDVAC) for CK_t/CK_c

Slew Rate [V/ns]	tDVAC [ps] @ $\|V_{IH/Ldiff(AC)}\|$ = 180mV		tDVAC [ps] @ $\|V_{IH/Ldiff(AC)}\|$ = 150mV		tDVAC [ps] @ $\|V_{IH/Ldiff(AC)}\|$ = 140 mV		tDVAC [ps] @ $\|V_{IH/Ldiff(AC)}\|$ = 130 mV	
	min	max	min	max	min	max	min	max
> 4.0	125	-	105	-	100	-	95	-
4.0	120	-	100	-	95	-	90	-
3.0	115	-	95	-	90	-	85	-
2.0	110	-	90	-	85	-	80	-
1.8	105	-	85	-	80	-	75	-
1.6	100	-	80	-	75	-	70	-
1.4	95	-	75	-	70	-	65	-
1.2	90	-	70	-	65	-	60	-
1.0	85	-	65	-	60	-	55	-
< 1.0	80	-	60	-	55	-	50	-

5.2.3 Single-ended requirements for CK_t/CK_c

Each individual component of the differential signal CK_t/CK_c has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach V_{SEH} min / V_{SEL} max (equal to the AC-levels ($V_{IH(AC)}$ / $V_{IL(AC)}$)) in every half-cycle.

Note that the applicable AC-levels for CK_t and CK_c are different per speed bin.

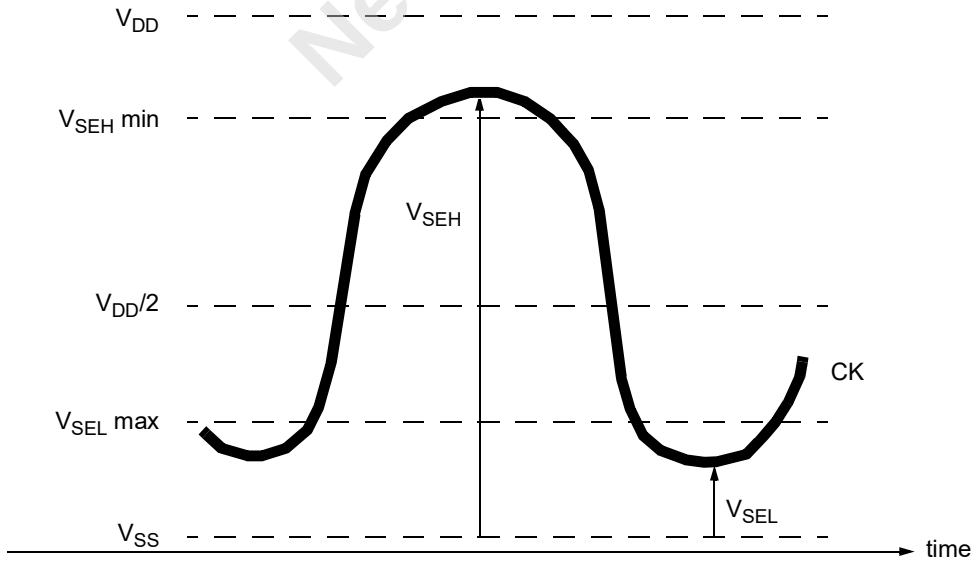


Figure 45 — Single-ended requirement for differential signals.

Note that, while ADD/CMD signal requirements are with respect to $V_{REF}CA$, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential

signals the requirement to reach V_{SEL} max, V_{SEH} min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 112 — Single-ended levels for CK_t/CK_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		Unit	NOTE
		Min	Max	Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK_t/CK_c	(V_{DD}/2) +90	NOTE 3	(V_{DD}/2) +75	NOTE 3	(V_{DD}/2) +70	NOTE 3	mV	1, 2
V_{SEL}	Single-ended low-level for CK_t/CK_c	NOTE 3	(V_{DD}/2) -90	NOTE 3	(V_{DD}/2) -75	NOTE 3	(V_{DD}/2) -70	mV	1, 2

Symbol	Parameter	DDR4-2933		DDR4-3200		Unit	NOTE
		Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK_t/CK_c	(V_{DD}/2) +65	NOTE 3	(V_{DD}/2) + 65	NOTE 3	mV	1, 2
V_{SEL}	Single-ended low-level for CK_t/CK_c	NOTE 3	(V_{DD}/2) -65	NOTE 3	(V_{DD}/2) - 65	mV	1, 2

NOTE 1: For CK_t/CK_c use $V_{IH.CA(AC)}$ / $V_{IL.CA(AC)}$ of ADD/CMD

NOTE2: $V_{IH(AC)}$ / $V_{IL(AC)}$ for ADD/CMD is based on VrefCA

NOTE 3: These values are not defined, however the single-ended signals CK_t /CK_c need to be within the limitations for overshoot and undershoot.

5.3 Differential Input Cross point voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 113. The differential input cross point voltage Vix is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.

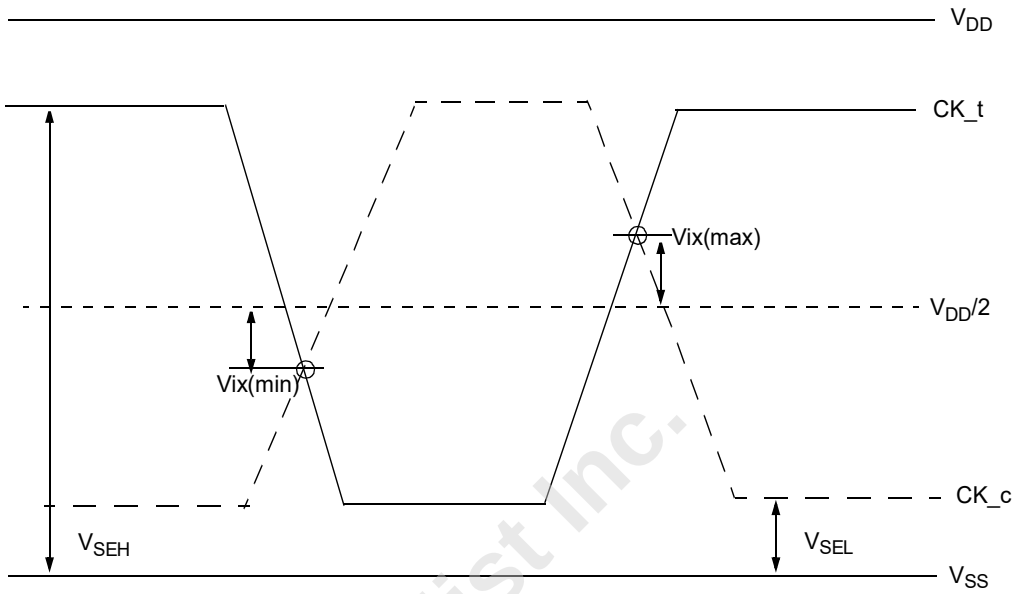


Figure 46 — Vix Definition (CK)

Table 113 — Cross point voltage for differential input signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133				Unit	NOTE
		min		max			
	Value of V_{SEH}, V_{SEL}	$V_{SEL} \le V_{DD}/2$ - 145	$V_{DD}/2$ - 145 ≤ $V_{SEL} \le V_{DD}/2$ - 90	$V_{DD}/2$ + 90 ≤ $V_{SEH} \le V_{DD}/2$ + 145	$V_{DD}/2$ + 145 ≤ V_{SEH}	mV	
V_{IX}(CK)	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK_t, CK_c	-120	-($V_{DD}/2$ - V_{SEL}) + 25	(V_{SEH} - $V_{DD}/2$) - 25	+120	mV	2
	Value of V_{SEH}, V_{SEL}	$V_{SEL} \le V_{DD}/2$ - 175	$V_{DD}/2$ - 175 ≤ $V_{SEL} \le V_{DD}/2$ - 90	$V_{DD}/2$ + 90 ≤ $V_{SEH} \le V_{DD}/2$ + 175	$V_{DD}/2$ + 175 ≤ V_{SEH}	mV	
V_{IX_EX}(CK)	Extended Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK_t, CK_c	-150	-($V_{DD}/2$ - V_{SEL}) + 25	(V_{SEH} - $V_{DD}/2$) - 25	+150	mV	1, 3

Symbol	Parameter	DDR4-2400/2666/2933/3200				Unit	NOTE
		min		max			
	Value of V_{SEH}, V_{SEL}	$V_{SEL} \le V_{DD}/2$ - 145	$V_{DD}/2$ - 145 ≤ $V_{SEL} \le V_{DD}/2$ - 75	$V_{DD}/2$ + 75 ≤ $V_{SEH} \le V_{DD}/2$ + 145	$V_{DD}/2$ + 145 ≤ V_{SEH}	mV	
V_{IX}(CK)	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK_t, CK_c	-120	-($V_{DD}/2$ - V_{SEL}) + 25	(V_{SEH} - $V_{DD}/2$) - 25	+120	mV	2
	Value of V_{SEH}, V_{SEL}	$V_{SEL} \le V_{DD}/2$ - 175	$V_{DD}/2$ - 175 ≤ $V_{SEL} \le V_{DD}/2$ - 75	$V_{DD}/2$ + 75 ≤ $V_{SEH} \le V_{DD}/2$ + 175	$V_{DD}/2$ + 175 ≤ V_{SEH}	mV	
V_{IX_EX}(CK)	Extended Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK_t, CK_c	-150	-($V_{DD}/2$ - V_{SEL}) + 25	(V_{SEH} - $V_{DD}/2$) - 25	+150	mV	1, 3

NOTE 1: Extended range for Vix is only allowed for clock, if single-ended clock input signals CK_t and CK_c are monotonic with a single-ended swing V_{SEL} / V_{SEH} of at least $V_{DD}/2$ +/- 50 mV, and when the differential slew rate of CK_t - CK_c is larger than 3 V/ns. Refer to Table 112 for V_{SEL} and V_{SEH} standard values.

NOTE 2: See Figure 71

NOTE 3: See Figure 73

5.4 Differential Input Slew Rate Definitions for CK

Input slew rate for differential signals CK_t/CK_c are defined and measured as shown in Table 114 and Figure 47.

Table 114 — Differential Input Slew Rate Definition for CK_t/CK_c

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t/CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTRdiff
Differential input slew rate for falling edge (CK_t/ CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	[$V_{IHdiffmin}$ - $V_{ILdiffmax}$] / DeltaTFdiff

NOTE1:The differential signal (i.e. CK_t/CK_c) must be monotonic between these thresholds

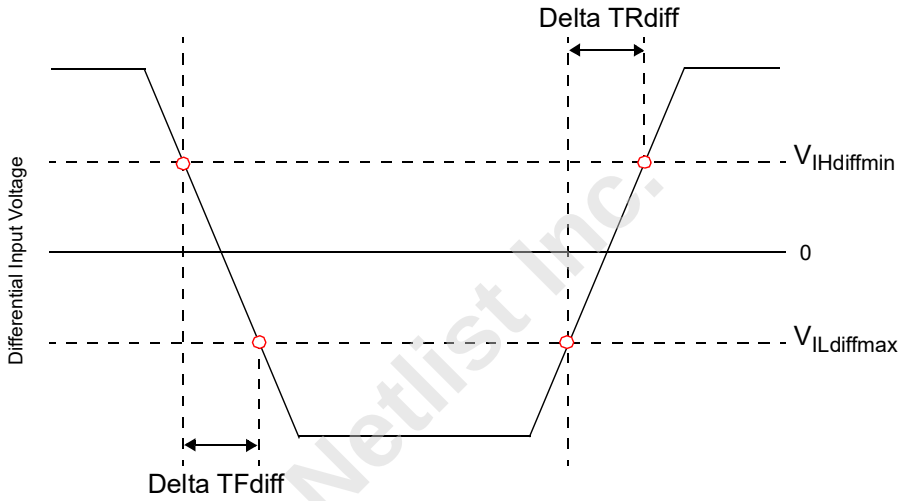


Figure 47 — Differential Input Slew Rate Definition for CK_t/CK_c

5.5 Input buffer characteristics

Table 115 — Input IBT characteristics over specified operating free-air temperature range

Symbol	Parameter	Conditions	Min	Max	Unit
$R_{IBT(tol)}$	Total Effective IBT Value Tolerance [1, 2]		-10	10	%
ΔV_M	Deviation of V_M w.r.t. $V_{DD}/2$ [3]	DA[17:0], DBA[1:0], DBG[1:0], DCKE[1:0], DODT[1:0], DPAR, DCS[n:0]_n, DC[2], DACT_n	-	2.5	%

1. Example for 100 Ω, Min = 90 Ω, Max = 110 Ω
2. Apply (V_{DD} + V_{IHL_ACmin})/2 to pin under test and measure current $I_{IH(AC)}$, then apply (V_{DD} - V_{IHL_ACmin})/2 to pin under test and measure current $I_{IL(AC)}$.
   R_{IBT} = (V_{IHL_ACmin})/($I_{IH(AC)}$ - $I_{IL(AC)}$)
3. Measure voltage (V_{OUT} = V_M) at test pin with no load (I_{OUT} = 0). ΔV_M = |2 *V_M/V_{DD} - 1| * 100%

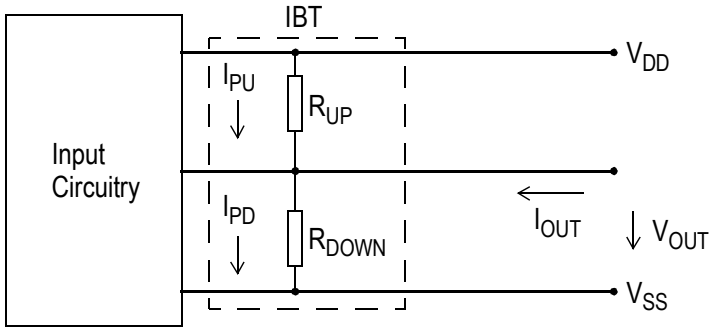


Figure 48 — Input Bus Termination: Definition of Voltages and Currents

5.6 CMOS Rail-to-Rail Input Levels for DRST_n

Table 116 — CMOS rail to rail Input Levels for DRST_n

Parameter	Symbol	Min	Max	Unit	NOTE
CMOS Input High Voltage	$V_{IH.CMOS}$	0.65 * V_{DD}	V_{DD}	V	1, 5
CMOS Input Low Voltage	$V_{IL.CMOS}$	V_{SS}	0.35 * V_{DD}	V	2, 6
Rise time	TR_RESET	-	1.0	µs	
DRST_n pulse width	$t_{INIT\_Power\_Stable}$	1.0	-	µs	3, 4

NOTE 1: Once DRST_n is registered HIGH, DRST_n level must be maintained above $V_{IH.CMOS,}$ otherwise, register operation will not be guaranteed until it is reset asserting DRST_n signal LOW.
NOTE 2: After DRST_n is registered LOW, DRST_n level shall be maintained below $V_{IL.CMOS}$ during tPW_RESET, otherwise, register may not be reset.
NOTE 3: DRST_n will clear all register settings to their default values.
NOTE 4: This definition only applies to “Reset Initialization with Stable Power”.
NOTE 5: Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
NOTE 6: Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

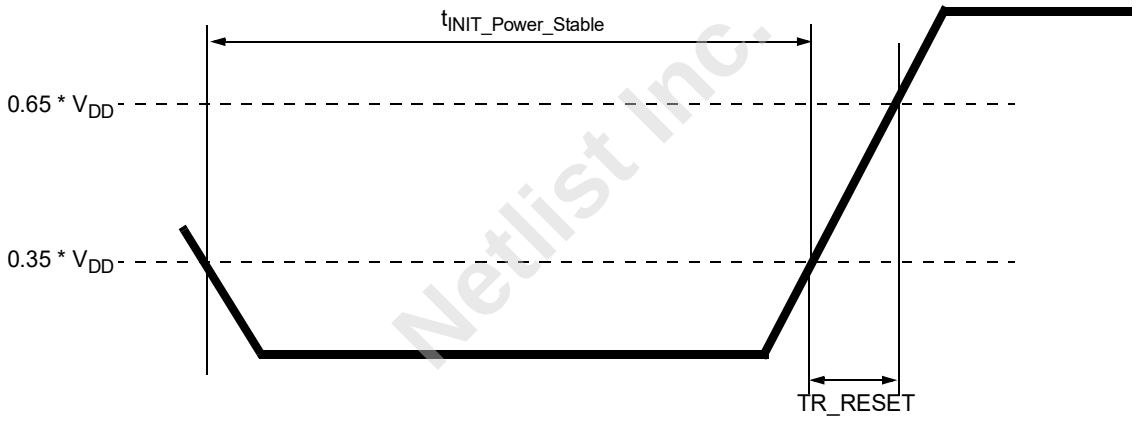


Figure 49 — DRST_n Input Slew Rate Definition

5.7 Overshoot and Undershoot Specifications

Table 117 — AC overshoot/undershoot specification for Address, Command and Control pins

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
Maximum peak amplitude above V_{DD} Absolute Max allowed for overshoot area	0.06	0.06	0.06	0.06	0.06	0.06	0.06	V
Delta value between V_{DD} Absolute Max and V_{DD} Max allowed for overshoot area	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	0.3	0.3	0.3	V
Maximum overshoot area per 1 t_{CK} above V_{DD} Absolute Max	0.0083	0.0071	0.0062	0.0055	0.0047	0.004	0.0034	V-ns
Maximum overshoot area per 1 t_{CK} between V_{DD} Absolute Max and V_{DD} Max	0.2550	0.2185	0.1914	0.1699	0.1505	0.1330	0.1180	V-ns
Maximum undershoot area per 1 t_{CK} below V_{SS}	0.2644	0.2265	0.1984	0.1762	0.1568	0.1375	0.1250	V-ns

NOTE 3: The AC overshoot/undershoot specification in Table 117 applies to pins DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DC0..DC2, DCS0/1_n, DCKE0/1, DODT0/1.

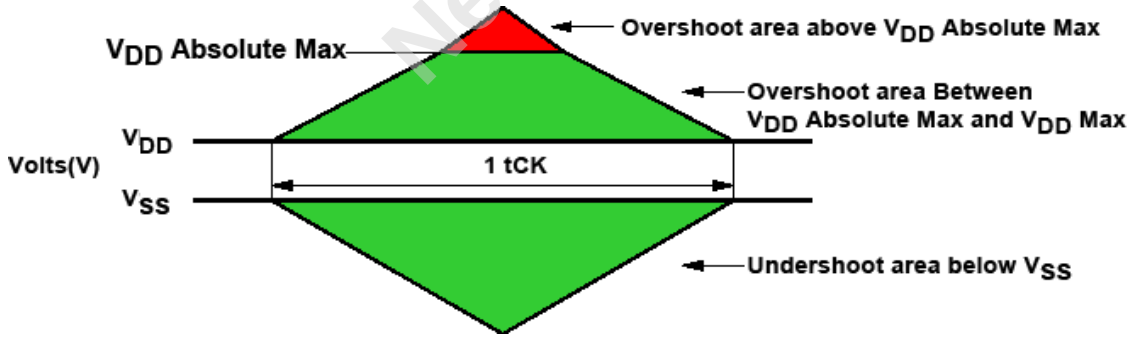


Figure 50 — Address, Command and Control Overshoot and Undershoot definition

Table 118 — AC overshoot/undershoot specification for Clock

Description	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
Maximum peak amplitude above V_{DD} Absolute Max allowed for overshoot area	0.16	0.16	0.16	0.16	0.16	0.16	0.16	V
Delta value between V_{DD} Absolute Max and V_{DD} Max allowed for overshoot area	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	0.3	0.3	0.3	V
Maximum overshoot area per 1 UI above V_{DD} Absolute Max	0.0150	0.0129	0.0113	0.0100	0.0090	0.0080	0.0080	V-ns
Maximum overshoot area per 1 UI between Absolute Max and V_{DD} Max	0.1050	0.090	0.0788	0.0700	0.0632	0.0575	0.0494	V-ns
Maximum undershoot below per 1 UI V_{SS}	0.1031	0.0884	0.0774	0.0688	0.0619	0.0563	0.0516	V-ns

NOTE 1: The AC overshot/undershoot specification in Table 118 applies to pins CK_t and CK_c

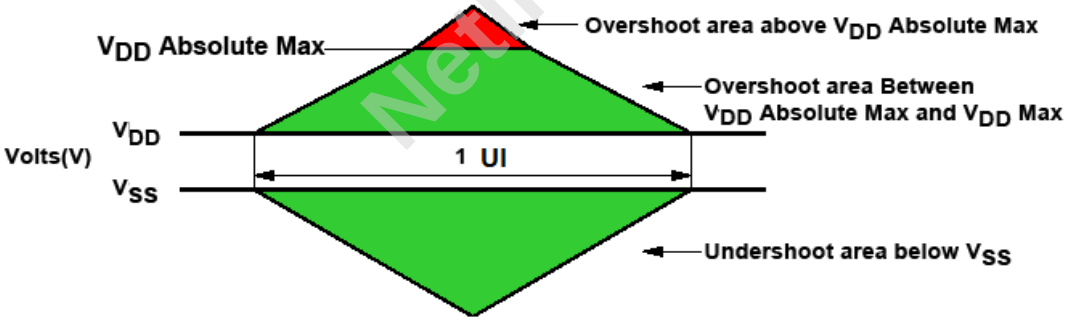


Figure 51 — Clock Overshoot and Undershoot definition

5.8 VrefCA Specifications

The internal VrefCA specifications parameters are Vref operating range, Vref step size, Vref set tolerance, Vref step time and Vref valid tolerance.

The Vref operating range specifies the minimum required Vref setting range for DDR4RCD02 devices and is specific by a Vref min operating point and a Vref max operating point, as depicted in Figure 52 below.

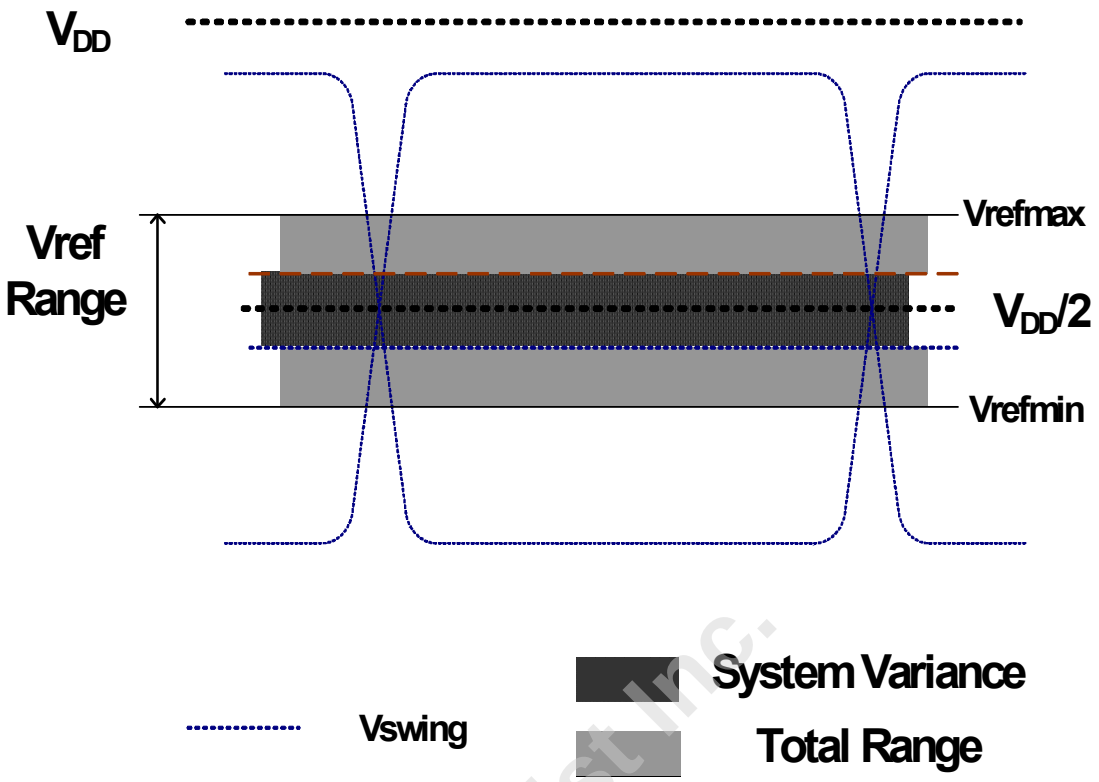


Figure 52 — Vref operating range(Vrefmin, Vrefmax)

The Vref step size is defined as the step size between adjacent steps. Vref step size ranges from 0.75% V_{DD} to 1.15% V_{DD}. However, for a given design, DDR4RCD02 has one value for Vref step size that falls within this range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two parameters for Vref set tolerance uncertainty for different numbers of steps n. The Vref set tolerance is measured with respect to the ideal line which is based on two endpoints, where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the step size and Vref set tolerance is below.

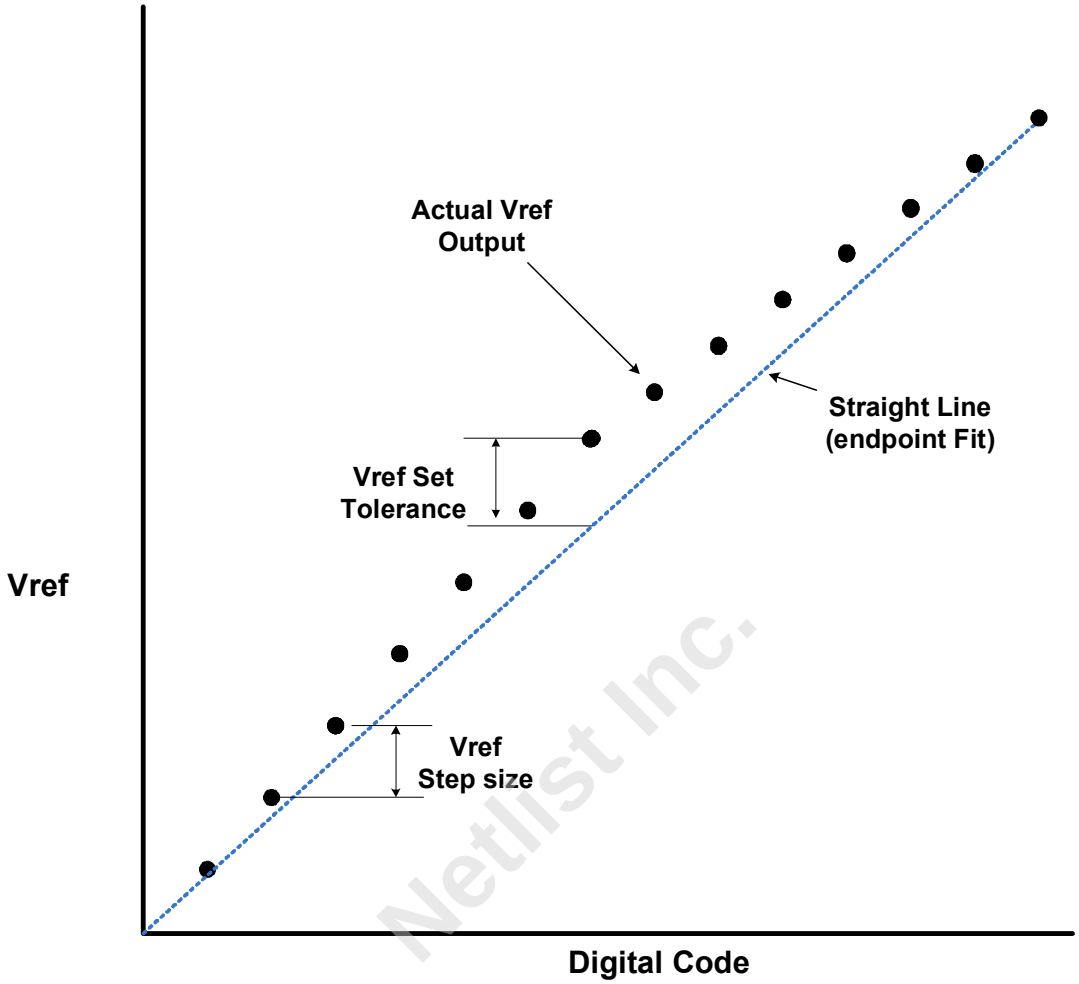


Figure 53 — Example of Vref set tolerance(max case only shown) and step size

The Vref increment/decrement step times are defined by Vref_time_short and Vref_time_long. Vref_time_short and Vref_time_long are defined from t0 to t1 as shown in the Figure 54 below where t0 is referenced to when the RCW write occurs and t1 is referenced to when the Vref voltage is at the final DC level within the Vref valid tolerance(Vref_val_tol).

The Vref valid level is defined by Vref_val_tol to qualify the step time t1 as shown in Figure 55. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for component level validation/characterization.

Vref_time_short is for a single step size increment/decrement change in Vref voltage.

Vref_time_long is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change in Vref voltage.

t0 - is referenced to RCW write command clock

t1 - is referenced to the Vref_val_tol

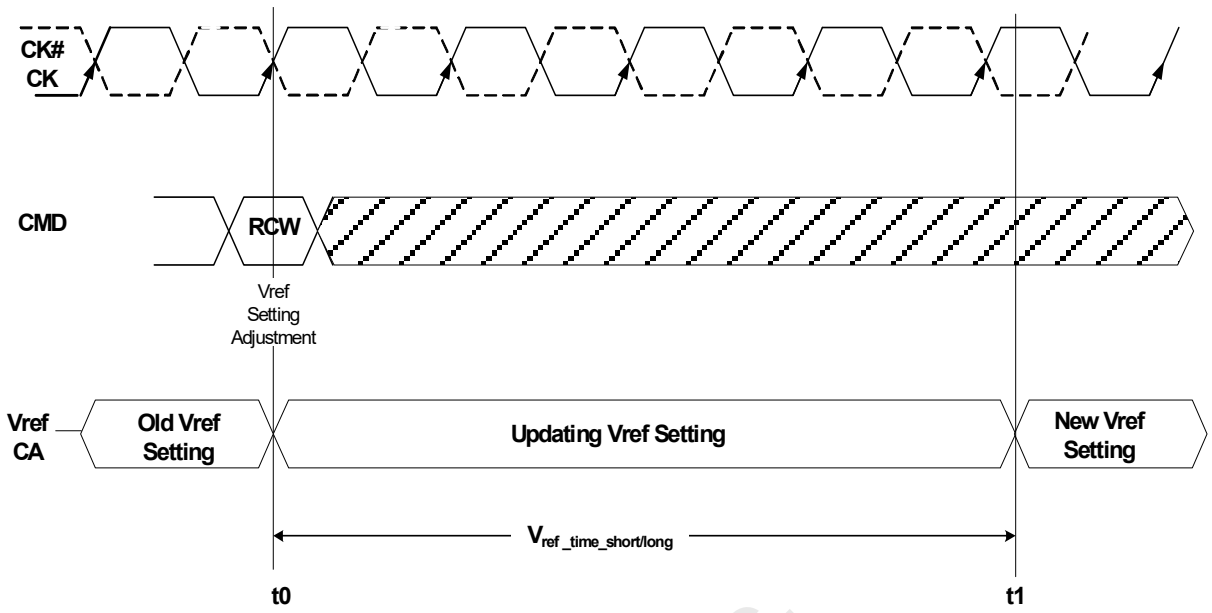


Figure 54 — Vref_time for short and long timing diagram

A RCW write to the F0RC1x (Internal Vref Control Word) is used to program the Vref value.

The minimum time required between two Vref RCW commands is Vref_time_short for single step and Vref_time_long for a full voltage range step.

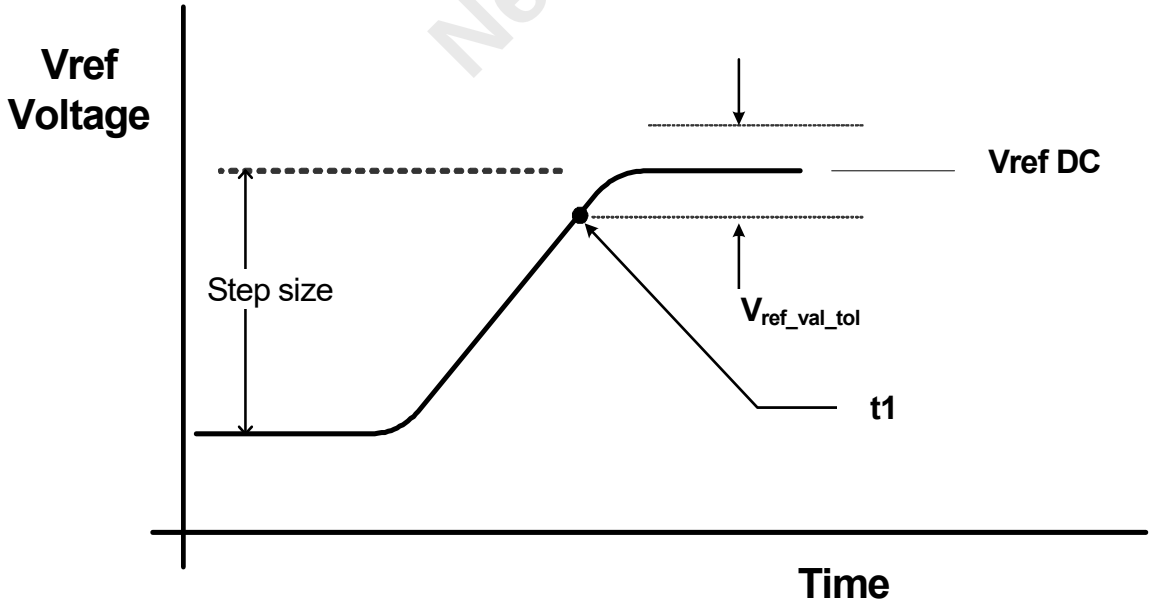


Figure 55 — Vref step single step size increment case

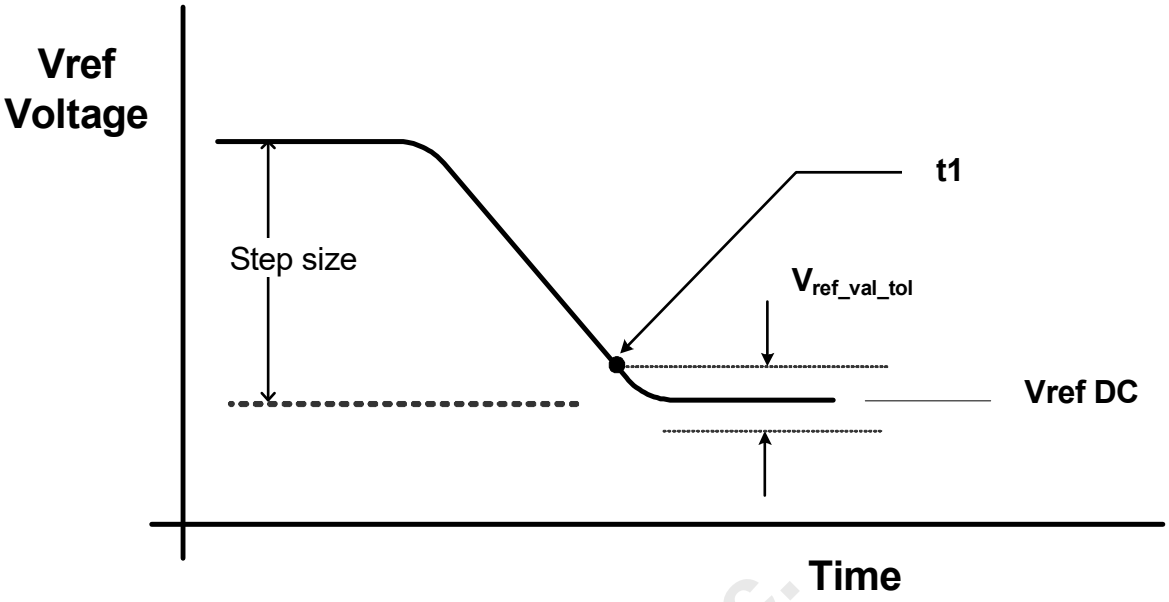


Figure 56 — Vref step single step size decrement case

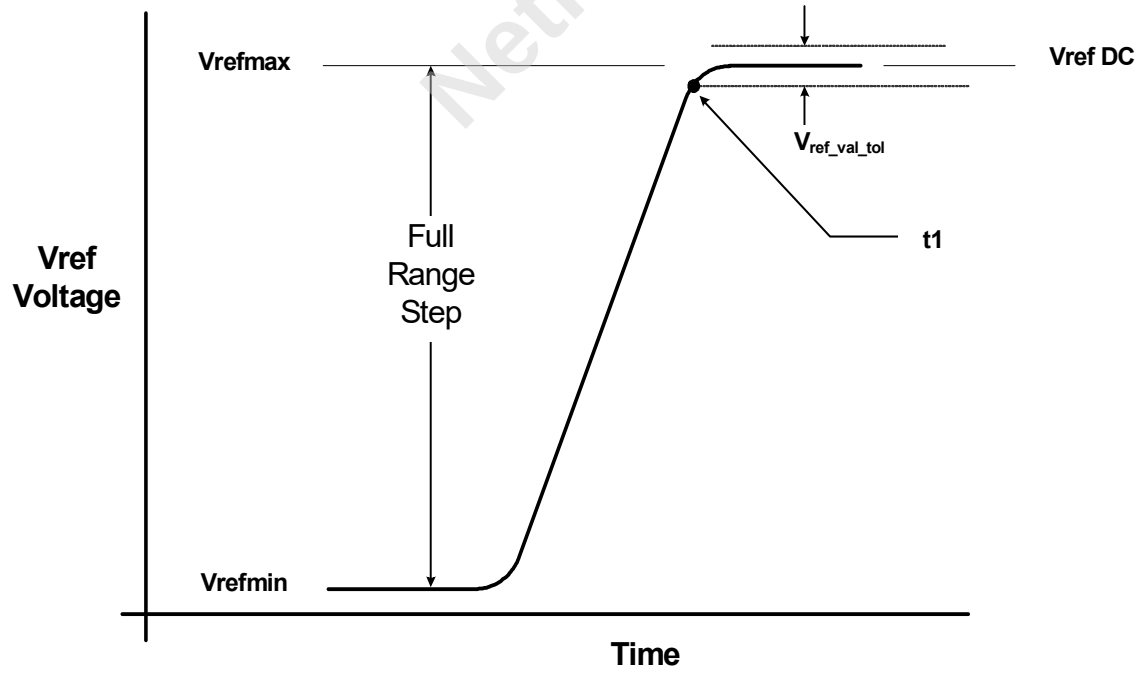


Figure 57 — Vref full step from Vrefmin to Vrefmax case

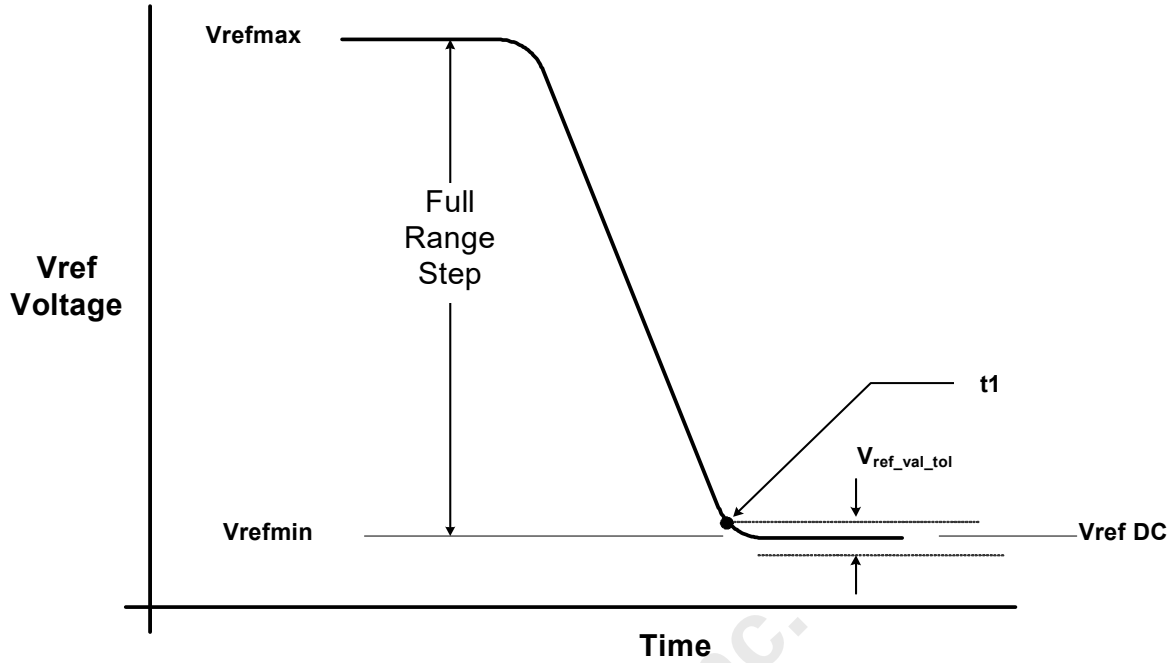


Figure 58 — Vref full step from Vrefmax to Vrefmin case

The table below contains the internal VrefCA specifications that will be characterized at the component level for compliance.

Table 119 — Internal VrefCA Specifications

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Vref Max Operating Point	Vref_max	67%	-		V_{DD}	
Vref Min Operating Point	Vref_min		-	33%	V_{DD}	
Vref Step size	Vref_step	0.75%		1.15%	V_{DD}	
	Vref_step(avg)	0.833%	-	Vref_step. max	V_{DD}	9
Vref Set Tolerance	Vref_set_tol_big	-2.0%	0.0%	2.0%	V_{DD}	1, 2, 4, 8
	Vref_set_tol_small	-0.2%	0.0%	0.2%	V_{DD}	1 , 3, 5
Vref Step Time	Vref_time_short	-	-	200	ns	6
	Vref_time_long	-	-	500	ns	7
Vref Valid Tolerance	Vref_val_tol	-0.2%	0.0%	0.2%	V_{DD}	8

NOTE 1: Vref_new = Vref_old +/- n*Vref_step; n=number of steps

NOTE 2: The minimum value of Vref setting tolerance = Vref_new - 2.0%*V_{DD}. The maximum value of Vref setting tolerance is Vref_new + 2.0%*V_{DD}. For n > 4.

NOTE 3: The minimum value of Vref setting tolerance = Vref_new - 0.2%*V_{DD}. The maximum value of Vref setting tolerance is Vref_new + 0.2%*V_{DD}. For n ≤ 4.

NOTE 4: Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line.

NOTE 5: Measured by recording the min and max values of the Vref output across four consecutive steps (n=4), drawing a straight line between those points and comparing all other Vref output settings to that line.

NOTE 6: Time from RCW write to increment or decrement one step size for Vref

NOTE 7: Time from RCW write to increment or decrement more than one step size up to full operating range for Vref
NOTE 8: Only applicable for component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
NOTE 9: Vref_step(avg) = (Vref_max - Vref_min)/ 40

Table 120 — QVrefCA and BVrefCA Specifications

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Vref Max Operating Point	Vref_max	67%	-		V_{DD}	
Vref Min Operating Point	Vref_min		-	33%	V_{DD}	
Vref Step size	Vref_step	0.75%		1.15%	V_{DD}	
	Vref_step(avg)	0.833%	-	Vref_step.max	V_{DD}	9
Vref Set Tolerance	Vref_set_tol_big	-3.0%	0.0%	3.0%	V_{DD}	1, 2, 4, 8
	Vref_set_tol_small	-0.3%	0.0%	0.3%	V_{DD}	1 , 3, 5
Vref Step Time	Vref_time_short	-	-	15	µs/µF	6, 10, 11
	Vref_time_long	-	-	50	µs/µF	7, 10, 11
Vref Valid Tolerance	Vref_val_tol	-0.3%	0.0%	0.3%	V_{DD}	8, 12

NOTE 1: Vref_new = Vref_old +/- n*Vref_step; n=number of steps
NOTE 2: The minimum value of Vref setting tolerance = Vref_new - 2.0%*V_{DD}. The maximum value of Vref setting tolerance is Vref_new + 2.0%*V_{DD}. For n > 4.
NOTE 3: The minimum value of Vref setting tolerance = Vref_new - 0.2%*V_{DD}. The maximum value of Vref setting tolerance is Vref_new + 0.2%*V_{DD}. For n ≤ 4.
NOTE 4: Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line.
NOTE 5: Measured by recording the min and max values of the Vref output across four consecutive steps (n=4), drawing a straight line between those points and comparing all other Vref output settings to that line.
NOTE 6: Time from RCW write to increment or decrement one step size for Vref
NOTE 7: Time from RCW write to increment or decrement more than one step size up to full operating range for Vref
NOTE 8: Only applicable for component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
NOTE 9: Vref_step(avg) = (Vref_max - Vref_min)/ 40
NOTE 10: See RDIMM specification for the amount of capacitance on the QVrefCA and BVrefCA nets.
NOTE 11: Changing the external QVrefCA and BVrefCA levels is only intended for module margining purposes, not as a means of power-up training.
NOTE 12: During power-up initialization the QVrefCA and BVrefCA outputs need to have valid $V_{DD}/2$ levels no later than step 7 in Figure 1

6 Output AC and DC Specifications

6.1 Single-Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single-ended signals as shown in Table 121 and Figure 59.

Table 121 — Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTFse
NOTE Output slew rate is verified by design and characterization, and may not be subject to production test.			

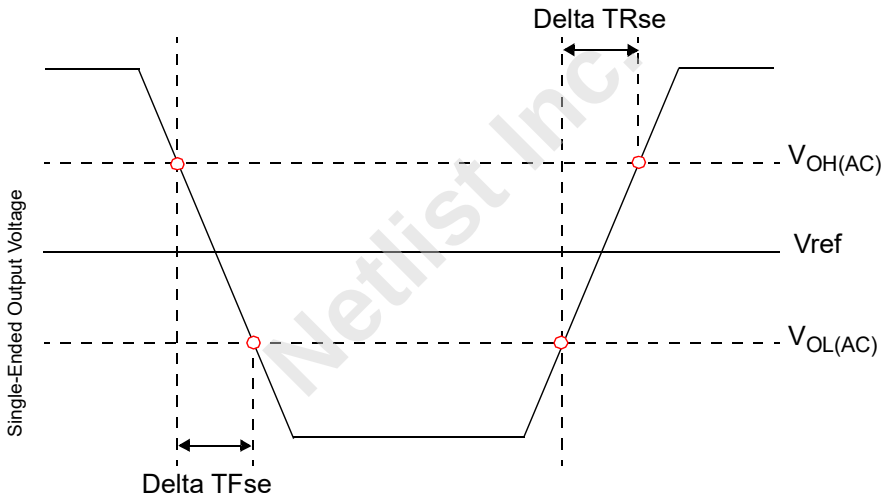


Figure 59 — Single-Ended Output Slew Rate Definition

Table 122 — Single-ended output edge rates over specified operating temperature range[1]

Symbol	Parameter	Conditions	DDR4-1600 to 2666		DDR4-2933		DDR4- 3200		Unit
			Min	Max	Min	Max	Min	Max	
dV/dt_r	rising edge slew rate[2]	1.2V operation	2	8	2	8	2	8	V/ns
dV/dt_f	falling edge slew rate[2]	1.2V operation	2	8	2	8	2	8	V/ns
$dV/dt\_f_{Alert\_n}$	falling edge slew rate[3]	1.2V operation	1	5	1	5	1	5	V/ns
dV/dt_D[4]	absolute difference between dV/dt_r and dV/dt_f		-	1	-	1	-	1	V/ns

1. These parameters are for the QxCA, BCOM, BODT, BCKE and outputs.

2. Measured into reference load in Figure 79
3. This is only for ALERT_n.falling edge slew rate. Measured at 0.75*V_{DD} +/- 0.15*V_{DD} into reference load in Figure 77
4. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

6.2 Differential Output Slew Rate Definitions for Yn_t / Yn_c and BCK_t / BCK_c

Output slew rates for differential signals Yn_t / Yn_c and BCK_t / BCK_c are defined and measured as shown in Table 123 and Figure 60.

Table 123 — Differential Output Slew Rate Definition for Yn_t / Yn_c and BCK_t / BCK_c

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge (Yn_t / Yn_c and BCK_t /BCK_c).	$V_{OLdiff(AC)}$	$V_{OHdiff(AC)}$	[$V_{OHdiff(AC)}$- $V_{OLdiff(AC)}$] / DeltaTRdiff
Differential output slew rate for falling edge (Yn_t / Yn_c and BCK_t /BCK_c).	$V_{OHdiff(AC)}$	$V_{OLdiff(AC)}$	[$V_{OHdiff(AC)}$ - $V_{OLdiff(AC)}$] / DeltaTFdiff
NOTE Differential output slew rate is verified by design and characterization, and may not be subject to production test.			

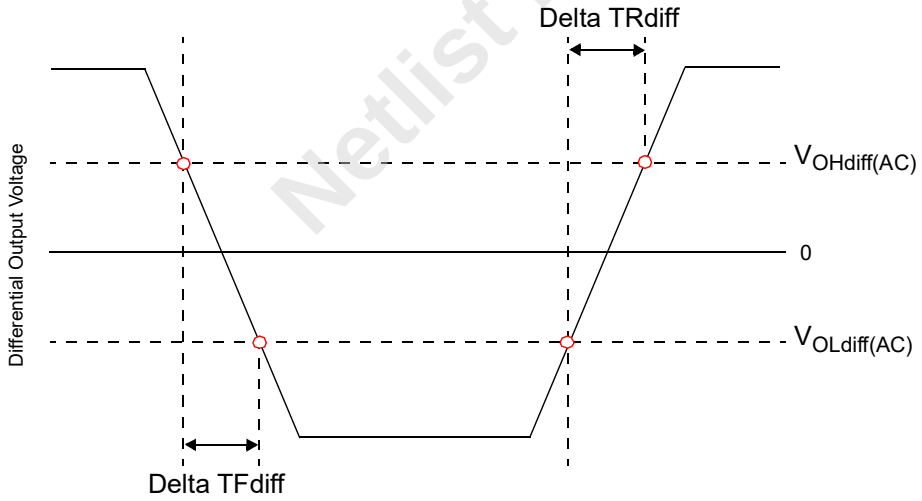


Figure 60 — Differential Output Slew Rate Definition for Yn_t / Yn_c and BCK_t / BCK_c

Table 124 — Differential output edge rates over specified operating temperature range[1]

Symbol	Parameter	Conditions	DDR4-1600 to 2666		DDR4-2933		DDR4-3200		Unit
			Min	Max	Min	Max	Min	Max	
dV/dt_r_diff	differential rising edge slew rate[2]	1.2V operation	4	16	4	16	4	16	V/ns
dV/dt_f_diff	differential falling edge slew rate[2]	1.2V operation	4	16	4	16	4	16	V/ns
dV/dt_D_diff[3]	absolute difference between dV/dt_r_diff and dV/dt_f_diff		-	2	-	2	-	2	V/ns

1. These parameters are for the Yn_t / Yn_c and BCK_t /BCK_c outputs.
2. Measured into reference load in Figure 79
3. Difference between dV/dt_r_diff (differential rising edge rate) and dV/dt_f_diff (differential falling edge rate)

6.3 Differential Output Cross Point Voltage

The differential cross point output voltage is defined as the max to min cross point measured on the differential signals Y[3:0]_t/Y[3:0]_c and BCK_t/BCK_c.

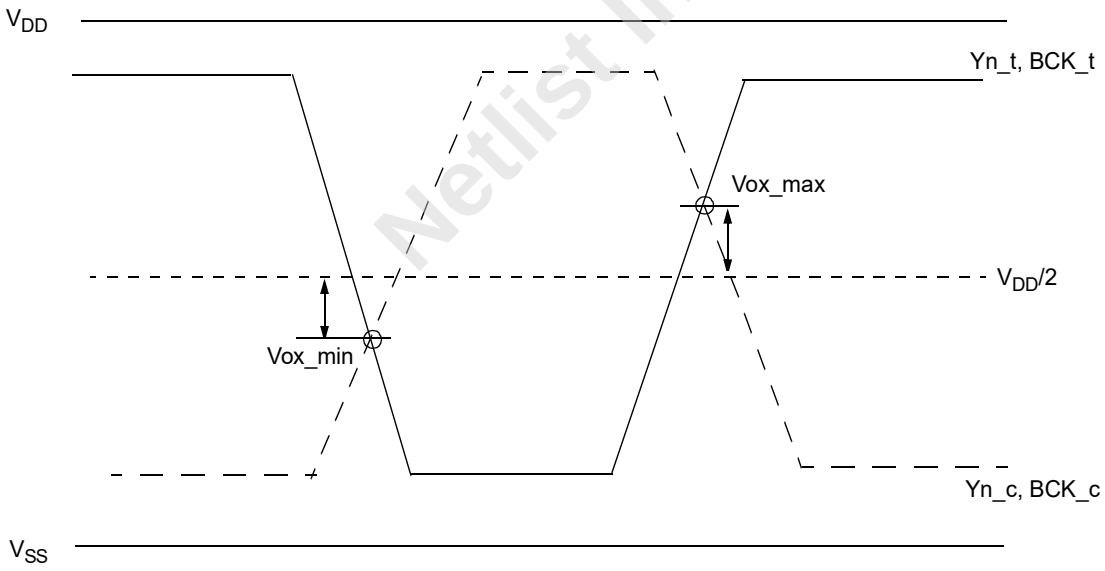


Figure 61 — Vox Definition (Yn and BCK)

Table 125 — Cross point voltage for Yn_t/Yn_c and BCK_t/BCK_c

Parameter	Symbol	DDR4-1600/ 1866/2133		DDR4-2400		DDR4-2666		DDR4-2933/ 3200		Unit	NOTE
		min	max	min	max	min	max	min	max		
Yn and BCK Differential output cross point voltage	Vox(clock)	-80	80	-70	70	-60	60	-50	50	mV	

6.4 Register R-on and Weak Drive Specifications for Each Drive Strength

Table 126 — Output Ron and Weak Drive

Symbol	Parameter	DDR4-1600 to 3200			Unit
		Min	Nom	Max	
ALERT_n					
$R_{on(ALERT)}$	ALERT_n Pull-down Impedance	see Table 127	16	see Table 127	Ω
BCOM[3:0]/BODT/BCKE/BCK_t/BCK_c					
$R_{on(BQM)}$	Moderate Drive Data Buffer Interface Drive Impedance[1]	see Table 127	RZQ[2]/12	see Table 127	Ω
$R_{on(BQS)}$	Strong Drive Data Buffer Interface Impedance[1]	see Table 127	RZQ[2]/17	see Table 127	Ω
QCMD/QADDR/QCTRL/Yn_t/Yn_c					
$R_{on(L)}$	Light Drive Impedance[1]	see Table 127	RZQ[2]/9	see Table 127	Ω
$R_{on(M)}$	Moderate Drive Impedance[1]		RZQ[2]/12		Ω
$R_{on(S)}$	Strong Drive Impedance[1]		RZQ[2]/17		Ω
$R_{on(VS)}$	Very Strong Drive Impedance[1]		RZQ[2]/24		Ω
$R_{on(W)}$	Weak Drive Impedance[1,3] for Light Drive		RZQ[2]/2		Ω
$R_{on(W)}$	Weak Drive Impedance[1,3] for Moderate Drive		RZQ[2]/3		Ω
$R_{on(W)}$	Weak Drive Impedance[1,3] for Strong Drive		RZQ[2]/3		Ω
$R_{on(W)}$	Weak Drive Impedance[1,3] for Very Strong Drive		RZQ[2]/4		Ω

NOTE 1: A functional representation of the output buffer is shown in Figure 62. Output impedance RON is defined by the value of the external reference resistor R_{ZQ} as defined in Table 127.

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{V_{DD} - V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pd} is turned off. (1)

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that RON_{Pu} is turned off.

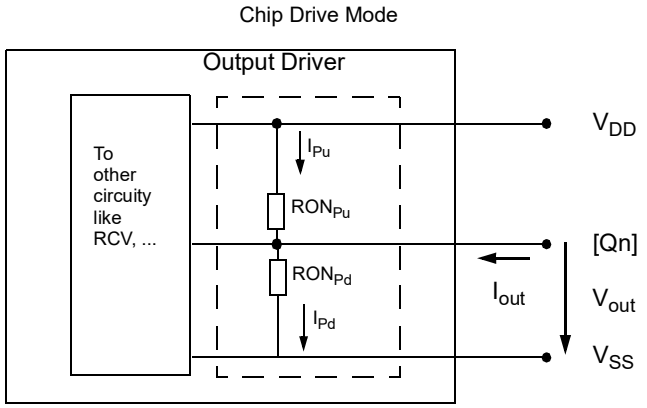


Figure 62 — Output Driver: Definition of Voltages and Currents

NOTE 2: Assuming R_{ZQ} = 240 Ω +/- 1%

NOTE 3: Output weak drive refers to allowing many A/B outputs to enter a state of higher output impedance when they are not being used. This is to conserve power when the outputs are resistively terminated to a voltage (e.g. V_{TT}).

Table 127 — Output Driver DC Electrical Characteristics, entire operating temperature range

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	NOTE
27 Ω	RON_{27Pd}	$V_{OLdc} = 0.2 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/9$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/9$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/9$	1, 2
	RON_{27Pu}	$V_{OLdc} = 0.2 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/9$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/9$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/9$	1, 2
20 Ω	RON_{20Pd}	$V_{OLdc} = 0.2 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/12$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/12$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/12$	1, 2
	RON_{20Pu}	$V_{OLdc} = 0.2 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/12$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/12$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/12$	1, 2
14 Ω	RON_{14Pd}	$V_{OLdc} = 0.2 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/17$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/17$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/17$	1, 2
	RON_{14Pu}	$V_{OLdc} = 0.2 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/17$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/17$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/17$	1, 2
10 Ω	RON_{10Pd}	$V_{OLdc} = 0.2 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/24$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/24$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/24$	1, 2
	RON_{10Pu}	$V_{OLdc} = 0.2 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/24$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/24$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/24$	1, 2

Table 127 — Output Driver DC Electrical Characteristics, entire operating temperature range

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	NOTE
16 Ω (for ALERT_n only)	RON_{16Pd}	$V_{OLdc} = 0.2 \times V_{DD}$	0.6	1.0	1.2	16 Ω	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.8	1.0	1.2	16 Ω	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.8	1.0	1.4	16 Ω	1, 2
120 Ω (weak drive only)	RON_{120Pd}	$V_{OLdc} = 0.2 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/2$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/2$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/2$	1, 2
	RON_{120Pu}	$V_{OLdc} = 0.2 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/2$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/2$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/2$	1, 2
80 Ω (weak drive only)	RON_{80Pd}	$V_{OLdc} = 0.2 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/3$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/3$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/3$	1, 2
	RON_{80Pu}	$V_{OLdc} = 0.2 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/3$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/3$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/3$	1, 2
60 Ω (weak drive only)	RON_{60Pd}	$V_{OLdc} = 0.2 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/4$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/4$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/4$	1, 2
	RON_{60Pu}	$V_{OLdc} = 0.2 \times V_{DD}$	0.85	1.0	1.4	$R_{ZQ}/4$	1, 2
		$V_{OMdc} = 0.5 \times V_{DD}$	0.85	1.0	1.15	$R_{ZQ}/4$	1, 2
		$V_{OHdc} = 0.8 \times V_{DD}$	0.6	1.0	1.15	$R_{ZQ}/4$	1, 2
Mismatch between pull-up and pull-down, MM_{PuPd}		$V_{OMdc} = 0.5 \times V_{DD}$	-10		10	%	1, 2, 3
Mismatch within component variation pull-up, MM_{Pudd}		$V_{OMdc} = 0.5 \times V_{DD}$	0		10	%	1, 2, 4
Mismatch within component variation pull-down, MM_{Pddd}		$V_{OMdc} = 0.5 \times V_{DD}$	0		10	%	1, 2, 4

Notes:
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see section on voltage and temperature sensitivity.
2. Pull-up and pull-down output driver impedances are recommended to be calibrated at 0.5 * V_{DD}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 * V_{DD} and 0.8 * V_{DD}.
3. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:
Measure RON_{Pu} and RON_{Pd}, both at 0.5 * V_{DD} separately; Ron-nom is the nominal Ron value:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x100$$

4. RON variance range ratio to RON nominal value in a given component

$$MM_{Pudd} = \frac{RON_{PuMax} - RON_{PuMin}}{RON_{Nom}} x100$$

$$MM_{Pddd} = \frac{RON_{PdMax} - RON_{PdMin}}{RON_{Nom}} x100$$

6.5 Output Driver and Termination Resistor Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration , the tolerance limits widen according to the Tables shown below.

.

Table 128 — Output Driver and Termination Resistor Sensitivity Definition

Resistor	Definition Point	Min	Max	Unit	Note
R_{ONPD}	0.5 x VDD	85 - ($dR_{ONPD}dT$ x $\|\Delta T\|$) - ($dR_{ONPD}dV$ x $\|\Delta V\|$)	115+($dR_{ONPD}dT$ x $\|\Delta T\|$) + ($dR_{ONPD}dV$ x $\|\Delta V\|$)	%	1,2
R_{ONPU}	0.5 x VDD	85 - (dR_{ONPU} x $\|\Delta T\|$) - (dR_{ONPU} x $\|\Delta V\|$)	115 +(dR_{ONPU} x $\|\Delta T\|$) + (dR_{ONPU} x $\|\Delta V\|$)	%	1,2
R_{IBT}	0.5 x VDD	90 - ($dR_{IBT}dT$ x $\|\Delta T\|$) - ($dR_{IBT}dV$ x $\|\Delta V\|$)	110 + ($dR_{IBT}dT$ x $\|\Delta T\|$) + ($dR_{IBT}dV$ x $\|\Delta V\|$)	%	1,2,3

Note.
1. ΔT = T - T(@ Calibration), ΔV = V - V(@ Calibration)
2. dRONPDdT, dRONPDdV, dRONPUdT, dRONPUdV, dRIBTdV, and dRIBTdT are not subject to production test but are verified by design and characterization.
3. This parameter applies to Input pin such as CK, CA and CS.

.

Table 129 — Output Driver and Termination Resistor Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
$dR_{ONPD}dT$	R_{ONPD} Temperature Sensitivity	0.00	0.2	%/°C
$dR_{ONPD}dV$	R_{ONPD} Voltage Sensitivity	0.00	0.15	%/mV
$dR_{ONPU}dT$	R_{ONPU} Temperature Sensitivity	0.00	0.2	%/°C
$dR_{ONPU}dV$	R_{ONPU} Voltage Sensitivity	0.00	0.15	%/mV
$dR_{IBT}T$	R_{IBT} Temperature Sensitivity	0.00	0.2	%/°C
$dR_{IBT}dV$	R_{IBT} Voltage Sensitivity	0.00	0.15	%/mV

6.6 ALERT_n Output Driver DC Electrical Characteristic

Table 130 — ALERT_n Output Driver DC Electrical Characteristics

Symbol	Parameter	Applicable Signals	Condition	Min	Nom	Max	Unit
I_{OL}	LOW-level output current ALERT_n	Measured at V_{OL} of 0.4V		20.8	-	-	mA
V_{OL}	Output LOW voltage ALERT_n	Measured at I_{OL} = 20.8 mA		-	-	0.4	V

6.7 Clock driver Characteristics

Table 131 — Clock driver Characteristics at application frequency (frequency band 1)

Symbol	Parameter	Conditions	DDR4-1600/ 1866/2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{jit(cc+)}$	Cycle-to-cycle period jitter		0	0.025 x t_{CK}	0	0.025 x t_{CK}	0	0.025 x t_{CK}	0	0.025 x t_{CK}	0	0.025 x t_{CK}	ps
$t_{jit(cc-)}$			0	0.025 x t_{CK}	0	0.025 x t_{CK}	0	0.025 x t_{CK}	0	0.025 x t_{CK}	0	0.025 x t_{CK}	ps
t_{STAB}	Stabilization time	CK_t/CK_c stable	-	5	-	5	-	5	-	5	-	5	µs
t_{CKsk}	Fractional Clock Output Skew[1]			10		10	-	10	-	10	-	10	ps
t_{jit}(per)	Yn Clock Period jitter		- 0.025 x t_{CK}	0.025 x t_{CK}	- 0.025 x t_{CK}	0.025 x t_{CK}	-0.025 x t_{CK}	0.025 x t_{CK}	-0.025 x tCK	0.025 x t_{CK}	-0.025 x tCK	-0.025 x tCK	ps
t_{jit}(hper)	Half period jitter		- 0.032 x t_{CK}	0.032 x t_{CK}	- 0.032 x t_{CK}	0.032 x t_{CK}	-0.032 x t_{CK}	0.032 x t_{CK}	-0.032 x t_{CK}	0.032 x t_{CK}	-0.032 x t_{CK}	0.032 x t_{CK}	ps
$t_{PW,H/L}$[2]	Yn_t/Yn_c Pulse Width duration		Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	Note 2	ns
t_{QSK1}[3]	Qn Output to clock tolerance		- 0.125 x t_{CK}	0.125 x t_{CK}	- 0.125 x t_{CK}	0.125 x t_{CK}	-0.1 x t_{CK}	0.1 x t_{CK}	-0.1 x t_{CK}	0.1x t_{CK}	-0.1 x t_{CK}	0.1x t_{CK}	ps
t_{staoff}[4]	Clock delay through the register between the input clock and output clock [5]		$t_{PDM(min)}$ + 1/2 * tCK	$t_{PDM(max)}$ + 1/2 * tCK	$t_{PDM(min)}$ + 1/2 * tCK	$t_{PDM(max)}$ + 1/2 * tCK	$t_{PDM(min)}$ + 1/2 * tCK	$t_{PDM(max)}$ + 1/2 * tCK	$t_{PDM(min)}$ + 1/2 * tCK	$t_{PDM(max)}$ + 1/2 * tCK	$t_{PDM(min)}$ + 1/2 * tCK	$t_{PDM(max)}$ + 1/2 * tCK	ns
t_{dynoff}[6]	Maximum re-driven dynamic clock offset[7]		-	50	-	45	-	45	-	40	-	40	ps

1. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 64). This parameter is specified for the clock pairs on each side of the register independently. The skew is applicable to right side clock pairs between Y0_t/Y0_c and Y2_t/Y2_c, as well as left side of the clock pairs between Y1_t/Y1_c and Y3_t/Y3_c. This is not a tested parameter and has to be considered as a design goal only.
2. t_{PW} = 0.5*t_{CK}-|t_{jit}(hper)min| to 0.5*t_{CK}+|t_{jit}(hper)max|
3. This skew represents the absolute Qn skew compared to the output clock Yn and contains the register pad skew, clock skew, package routing skew and SSO noise (See Figure 65). The output clock jitter is included in this skew. The Qn output can be either early or late. For outputs QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR, QxCKE0/1, QxODT0/1, QxC2, QxCS[1:0]_n for Dual CS mode, QxCS[3:0] this parameter applies to each side of the register independently. This parameter also applies to the BCOM[3:0], BCKE and BODT outputs w.r.t. to the output clock BCK.
4. F0RC0A must be set to correct speed and the device must run at one of the speed nodes defined in Table 141. See Figure 63.
5. This measures the delay from the rising differential input clock which samples incoming C/A to the rising differential output clock that will be used to sample the same C/A data. The parameter describes the maximum and minimum Yn clock t_{PD} .
6. V_{DD} measurement DC bandwidth is limited to 20MHz.
7. See Figure 63.

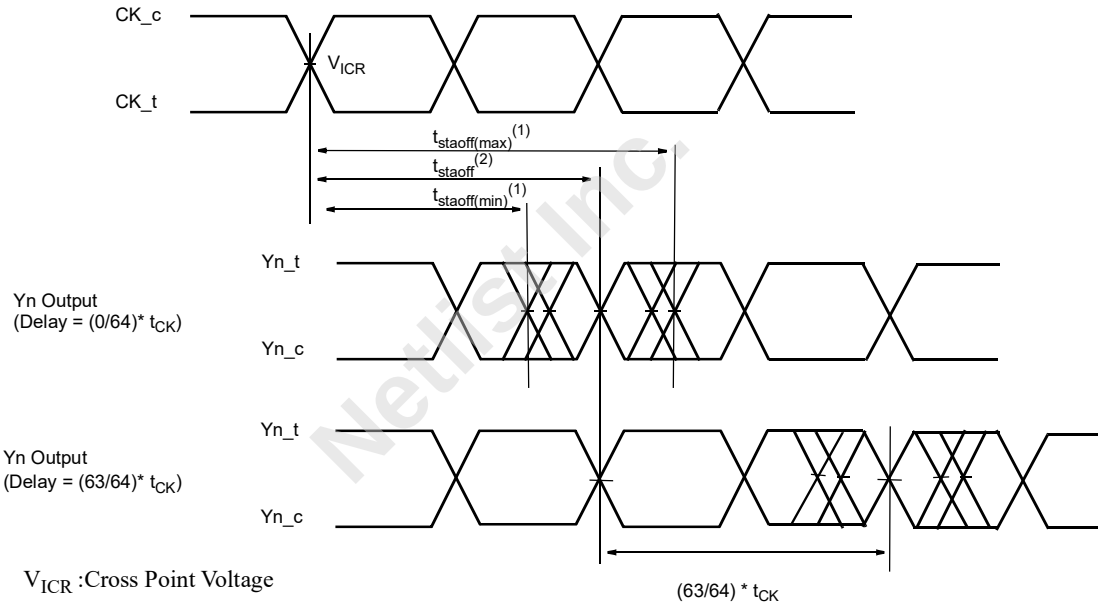


Figure 63 — Definition for tstaoff and tdynoff

1. $t_{staoff(max/min)}$ = propagation delay specification limits for clock signal (rising CK input clock edge to rising Yn output clock edge for corresponding data cycles) over process, voltage and temperature
2. t_{staoff} = measured propagation delay for clock signal (rising CK input clock edge to rising Yn output clock edge for corresponding data cycles)
3. t_{dynoff} = maximum propagation delay variation over voltage and temperature within t_{staoff} window. This includes all sources of jitter and drift (e.g. thermal noise, supply noise, voltage/temperature drift, SSC tracking, SSO, etc) except reference clock noise.

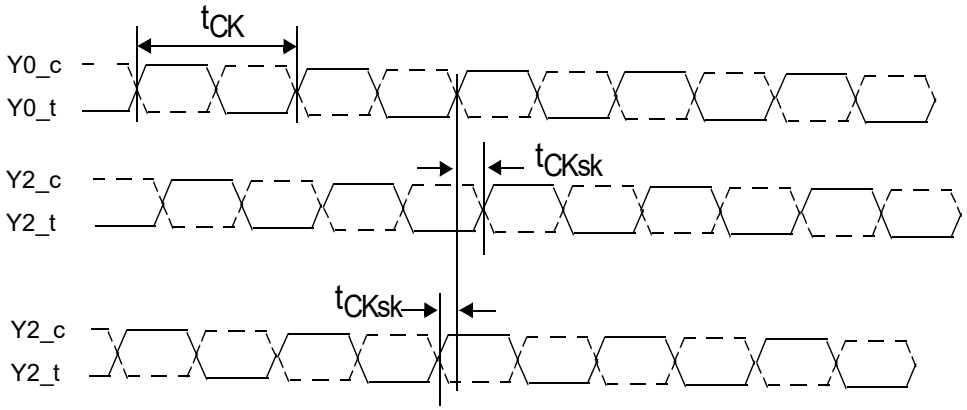


Figure 64 — Clock Output (Yn) Skew

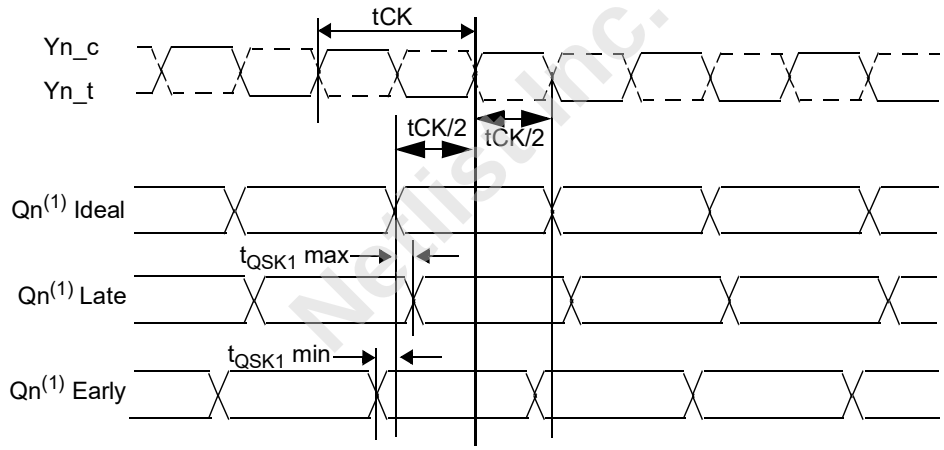


Figure 65 — Qn Output Skew

1. Outputs as specified in Table 131, “Clock driver Characteristics at application frequency (frequency band 1),” Footnote 3

Table 132 — Clock driver Characteristics at test frequency (frequency band 2)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{jit}(cc)$	Cycle-to-cycle period jitter		0	160	ps
t_{STAB}	Stabilization time		-	15	µs

Table 132 — Clock driver Characteristics at test frequency (frequency band 2)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{CKsk}	Total Clock Output Skew[1]			100	ps
	Fractional Clock Output skew[2]			vs[3]	ps
t_{jit}(per)	Yn Clock Period jitter		-160	160	ps
t_{jit}(hper)	Half period jitter		-200	200	ps
t_{QSK1}[4]	Qn Output to clock tolerance (Standard 1/2-Clock Pre-Launch)		-100	vs[3]	ps
t_{dynoff}	Maximum re-driven dynamic clock offset[5]		-500	500	ps

1. This skew represents the absolute output clock skew and contains the pad skew and package skew.
2. This skew represents the absolute output clock skew and contains the pad skew and package skew (See Figure 64, “Clock Output (Yn) Skew” on page 152)
3. Vendor Specific
4. -This skew represents the absolute Qn skew compared to the output clock (Yn), and contains the register pad skew, clock skew and package routing skew (See Figure 65, “Qn Output Skew” on page 152). The output clock jitter is not included in this skew. This parameter applies to each side of the register independently. The parameter includes the skew related to simultaneous switching noise (SSO). The Qn output can either be early or late.
5. -The re-driven clock signal is ideally centered in the address/control signal eye. This parameter describes the dynamic deviation from this ideal position including jitter and dynamic phase offset.

Table 133 — SSC and PLL Loop Filter Characteristics

Symbol	Parameter	Conditions	DDR4-1600/1866/2133/2400/2666/2933/3200		Unit
			Min	Max	
f_{SSC}	SSC modulation frequency[1]		30	33	kHz
a_{SSC}	SSC amplitude[1]		0	-0.5	%
f_{band}	PLL loop bandwidth[2]	-3dB bandwidth[3]	0.05 x f_{clock}	-	MHz

1. The DDR4RCD02 must meet all parameters defined in this specification while supporting input clock SSC requirements described in this table
2. The DDR4RCD02 PLL must fulfill this loop filter requirement in order to track typical system clock synthesizer output clock signals
3. Implies a jitter peaking of <3 dB

7 DC specifications, IDD Specifications

7.1 DC Electrical Characteristics

Table 134 — DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	Input current	DRST_n, $V_I = V_{DD}$ or V_{SS}	-	-	± 5	µA
I_{ID}	Input current	Data inputs[1], $V_I = V_{DD}$ or V_{SS}	-	-	± 5	µA
I_{ID}	Input current	CK_t, CK_c[2]; $V_I = V_{DD}$ or V_{SS}	-5		150	µA

1. DCKE0/1, DODT0/1, DA0 .. DA17, DBA0 .. DBA1, DBG0 .. DBG1, DACT_n, DC0 .. DC2, DPAR, DCS0/1_n are measured while DRST_n pulled LOW.
2. The CK_t and CK_c inputs have internal pull-down resistors in the range of 10 kΩ to 100 kΩ.

7.2 IDD Specification Parameters and Test Conditions

In this chapter, IDD measurement conditions such as test load and patterns are defined. Figure 66 shows the setup and test load for IDD measurements.

- IDD currents (such as IDD3N, IDD3P, IDD4A, IDD4B, IDD6R and IDD6S) are measured as time-averaged currents with all V_{DD} balls of the DDR4RCD02 under test tied together.
- IDD currents can be measured for each speed bin. Each measurement shall use the minimum tCK (avg) for each speed bin as specified in Table 117 of the DDR4DB02 specification.
- **ATTENTION:** IDD values cannot be directly used to calculate IO power of the DDR4RCD02. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 67.

For IDD measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} <= V_{IL(AC)}$.max.
- "1" and "HIGH" is defined as $V_{IN} >= V_{IH(AC)}$.min.
- "MID-LEVEL" is defined as inputs are Vref = V_{DD} / 2.
- Basic IDD Measurement Conditions are described in Table 135.
- Detailed IDD Measurement-Loop Patterns are described in Table 136 through Table 138.
- IDD Measurements are done after properly initializing the DDR4RCD02. This includes but is not limited to setting
  Weak drive is enabled in F0RC00;
  All four clock outputs enabled in F0RC01;
  DA17 and DPAR IBT enabled in F0RC02;
  Moderate drive strength ('0101') in F0RC03, F0RC04, F0RC05;
  QxC[2:0], QxPAR and QxA17 outputs enabled in F0RC08;
  DCS1 IBT and QxCS1_n outputs enabled in F0RC09;
  CKE Power Down Mode is enabled in F0RC09;
  Parity checking disabled in F0RC0E;
  I^2C Bus interface enabled in F0RC2x;
  100 Ω IBT enabled for CA, DCS[3:0]_n, DCKE and DODT in F0RC7x;
  DC[2:0] and DCKE1 IBT and DCKE1 input and QxCKE1 outputs enabled in F0RCBx

- **ATTENTION:** The IDD Measurement-Loop Patterns need to be executed at least one time before actual IDD measurement is started.
- Define D = {DCS[1:0]_n, DACT_n, DRAS_n, DCAS_n, DWE_n } := {HIGH, HIGH, LOW, LOW, LOW, LOW}
- Define D# = {DCS[1:0]_n, DACT_n, DRAS_n, DCAS_n, DWE_n } := {HIGH, HIGH, HIGH, HIGH, HIGH, HIGH}

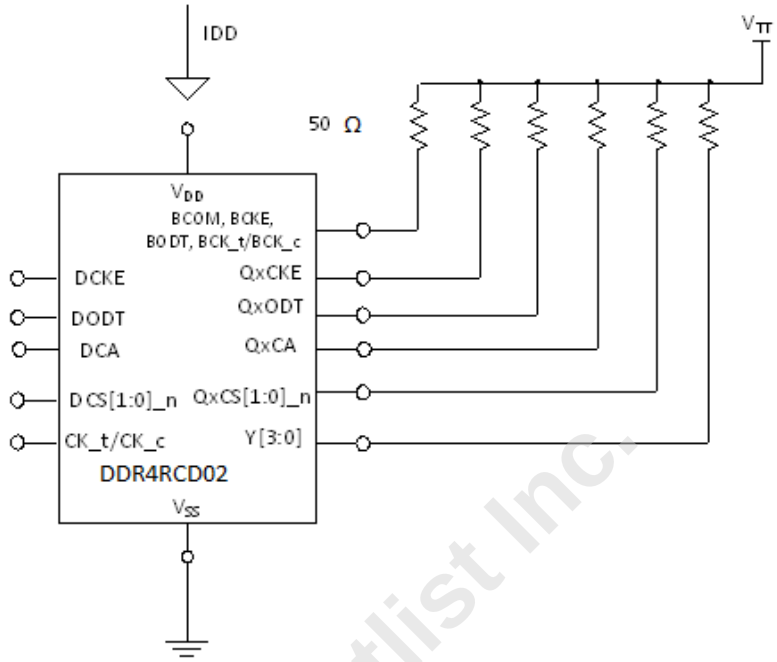


Figure 66 — Measurement Setup and Test Load for IDD Measurements

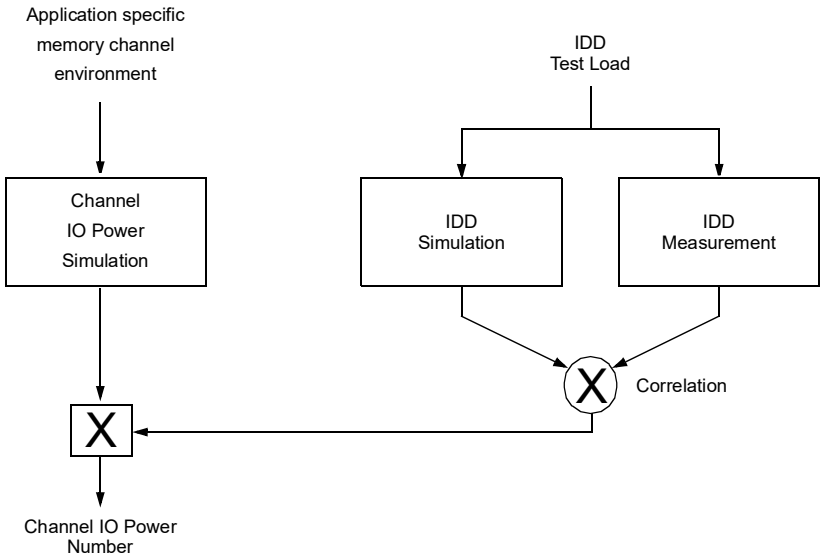


Figure 67 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDD Measurement

Table 135 — Basic IDD Measurement Conditions

Symbol	Description
IDD3N	**Active Idle Current** **DB interface:** Disabled **DCKE**: HIGH; **External clock:** On; **Data IO:** see Table 136 on page 156; **Pattern Details:** see Table 136 on page 156 **QxCA, QxCKE, QxODT, Y[3:0]** termination is 50 Ω to V_{TT}
IDD3P1	**CKE Power Down with IBT On Current** **DB interface:** Enabled; **CKE Power Down Mode:** IBT On (F0RC09 DA3:2 = 10) **DCKE**: LOW **External clock:** On; **Data IO:** see Table 136 on page 156; **Pattern Details:** see Table 137 on page 156 **QxCA, QxCKE, QxODT, Y[3:0]** termination is 50 Ω to V_{TT}
IDD3P2	**CKE Power Down with IBT Off Current** **CKE Power Down Mode:** IBT Off (F0RC09 DA3:2 = 11); **Pattern Details:** see Table 137 on page 156 **Other conditions:** see IDD3P1
IDD4A	**Active Current with DB interface disabled** **DCKE:** HIGH; **External clock:** On; **Pattern Details:** see Table 138 on page 157 **QxCA, QxCKE, QxODT, Y[3:0]** termination is 50 Ω to V_{TT}
IDD4B	**Active Current with DB interface enabled** **DCKE:** HIGH; **External clock:** On; **Pattern Details:** see Table 138 on page 157 **QxCA, QxCKE, QxODT, Y[3:0], BCOM, BODT, BCKE & BCK_t/BCK_c** termination is 50 Ω to V_{TT}
IDD6R	**Static Reset Current** **DRST_n:** LOW; **External clock:** Off; CK_t and CK_c: LOW; **DCKE**: LOW Outputs tri-stated (except QxCKE = LOW, BCKE = HIGH); **QxCKE & BCKE** termination is 50 Ω to V_{TT}
IDD6S	**Clock Stopped Power Down Current** **DRST_n:** HIGH; **External clock:** Off; CK_t and CK_c: LOW; **DCKE**: LOW Outputs tri-stated (except QxCKE = BCKE = LOW); **QxCKE & BCKE** termination is 50 Ω to V_{TT}

Table 136 — IDD3N Measurement-Loop Pattern

CK_t, CK_c	DCKE[1:0]	Cycle Number	Command	DCS[1:0]_n	DACT_n	DRAS_n/DA16	DCAS_n/DA15	DWE_n/DA14	DODT[1:0]	DC[2:0]	DBG[1:0]^2	DBA[1:0]	DA12/BC_n	DA[17,13,11]	DA[10]/AP	DA[9:7]	DA[6:3]	DA[2:0]
toggling	Static HIGH	0	D, D	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	D, D	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		2	D#, D#	3	1	1	1	1	0	0	3	3	0	0	0	7	F	0
		3	D#, D#	3	1	1	1	1	0	0	3	3	0	0	0	7	F	0

Table 137 — IDD3P1 and IDD3P2 Measurement-Loop Pattern

CK_t, CK_c	DCKE[1:0]	Cycle Number	Command	DCS[1:0]_n	DACT_n	DRAS_n/DA16	DCAS_n/DA15	DWE_n/DA14	DODT[1:0]	DC[2:0]	DBG[1:0]^2	DBA[1:0]	DA12/BC_n	DA[17,13,11]	DA[10]/AP	DA[9:7]	DA[6:3]	DA[2:0]
toggling	Static LOW	0	D, D	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	D, D	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		2	D#, D#	3	1	1	1	1	0	0	3	3	0	0	0	7	F	0
		3	D#, D#	3	1	1	1	1	0	0	3	3	0	0	0	7	F	0

Table 138 — IDD4A, IDD4B Measurement-Loop Pattern

CK_t, CK_c	DCKE[1:0]	Sub-Loop	Cycle Number	Command	DCS[1:0]_n	DACT_n	DRAS_n/DA16	DCAS_n/DA15	DWE_n/DA14	DODT[1:0]	DC[2:0]	DBG[1:0]	DBA[1:0]	DA12/BC_n	DA[17,13,11]	DA[10]/AP	DA[9:7]	DA[6:3]	DA[2:0]
toggling	Static HIGH	0	0	**RD**	2	1	1	0	1	0	0	0	0	0	0	0	0	0	0
			1	D	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	D, D	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			3	D, D	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	4	**RD**	1	1	1	0	1	0	0	3	3	0	0	0	7	F	0
			5	D#, D#	3	1	1	1	1	0	0	3	3	0	0	0	7	F	0
			6	D#, D#	3	1	1	1	1	0	0	3	3	0	0	0	7	F	0
			7	D#, D#	3	1	1	1	1	0	0	3	3	0	0	0	7	F	0

8 Input/Output Capacitance

Table 139 — Silicon pad I/O Capacitance values

Symbol	Parameter	Conditions	DDR4-1600/ 1866/2133		DDR4-2400/ 2666/2933		DDR4 - 3200		Unit
			Min	Max	Min	Max	Min	Max	
C_I	Input capacitance, Data inputs	see footnote[1,2]	0.8	1.1	0.8	1.0	0.8	1.0	pF
C_O	Output capacitance		1.5	3.5	1.5	3.5	1.5	3.5	pF
C_{CK}	Input capacitance, CK_t, CK_c	see footnote[1,2]	0.8	1.1	0.8	1.0	0.8	1.0	pF
C_{DCK}	Input capacitance delta CK_t and CK_c	see footnote[1,3]	-	0.1	-	0.1	-	0.1	pF
C_{ID}	Delta capacitance over all inputs		-	0.2	-	0.2	-	0.2	pF
C_{IR}	Input capacitance, DRST_n	$V_I = V_{DD}$ or V_{SS}; V_{DD} = 1.2 V	0.5	2	0.5	2	0.5	2	pF
C_{ALERT}	Output capacitance of ALERT_n		0.5	2	0.5	2	0.5	2	pF
C_{ERROR_IN}	Input capacitance of ERROR_IN_n		0.5	2	0.5	2	0.5	2	pF

1. This parameter does not include package capacitance
2. Data inputs are DCKE0/1, DODT0/1, DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DC0 .. DC2, DPAR, DCS0/1_n
3. Absolute value CK_t - CK_c

Table 140 — Package electrical specifications

Symbol	Parameter	DDR4-1600 to3200		Unit	Notes
		Min	Max		
$Z_{I\ CTRL}$	Input CTRL pins Zpkg	45	75	Ω	1, 2, 4
$Td_{I\ CTRL}$	Input CTRL pins Pkg Delay	14	50	ps	1, 3, 4
DTd_{ICTRL}	Delta CTRL pins Pkg Delay	-	20	ps	1,3, 4
ZI_{CA}	Input CA pins Zpkg	45	75	Ω	1, 2, 5
Td_{CAI}	Input CApins Pkg Delay	14	50	ps	1, 3, 5
DTd_{CAI}	Delta CA input pins Pkg Delay	-	20	ps	1, 3, 5
ZO_{CA}	Output CA pins Zpkg	45	75	Ω	1, 2, 9
Td_{CAO}	Output CA pins Pkg Delay	14	50	ps	1, 3, 9
DTd_{CAO}	Delta CA output pins Pkg Delay	-	20	ps	1, 3, 9
ZO_{DB}	Output DB pins Zpkg	45	75	Ω	1, 3, 13
Td_{DBO}	Output DB pins Pkg Delay	14	50	ps	1, 3, 13
DTd_{DBO}	Delta DB output pins Pkg Delay	-	20	ps	1, 3, 13
ZI_{CK}	Input CK pins ZPkg	40	70	Ω	1, 2, 8
Td_{CKI}	Input CK pins Pkg Delay	14	50	ps	1, 3
ZO_{Y}	Output Yn pins ZPkg	40	70	Ω	1, 2, 8
Td_{Y}	Output Yn pins Pkg Delay	14	50	ps	1, 3
DTd_{Y}	Delta Delay between Y0_t, Y1_t, Y2_t and Y3_t	-	20	ps	12
DZ_{DCK}	Delta Zpkg CK_t and CK_c	-	10	Ω	1, 2, 6
DTd_{DCK}	Delta Delay CK_t and CK_c	-	5	ps	1, 3, 7
DZ_{DY}	Delta Zpkg Yn_t and Yn_c	-	10	Ω	1, 2, 10
DTd_{DY}	Delta Delay Yn_t and Yn_c	-	5	ps	1, 3, 11
$Z_{O\ ZQ}$	Output ZQCAL Zpkg	30	70	Ω	1, 2
$Z_{O\ ALERT}$	Output ALERT_n Zpkg	30	100	Ω	1, 2
$Td_{O\ ALERT}$	Output ALERT_n Pkg Delay	10	55	ps	1, 3

NOTE 1: This parameter is not subject to production test. It is verified by design and characterization. The package parasitics (L &C) are determined using package only samples. Package capacitance and inductance are computed from S-parameters. The capacitance is derived with V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, PV_{DD}, PV_{SS} shorted and all other signals floating. The inductance is derived with V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, PV_{DD}, PV_{SS} shorted and all other signals shorted at the die side (not pin).

NOTE 2: Package only impedance (Zpkg) is calculated based on the computed Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT(Lpkg/Cpkg)

NOTE 3: Package only delay (Tdpkg) is calculated based on computed Lpkg and Zpkg total for a given pin where: Tdpkg (total per pin) = SQRT(Lpkg*Cpkg)

NOTE 4: This value applies to DCKE0/1, DODT0/1, DCS0_n .. DCS3_n

NOTE 5: This value applies to DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DC2, DPAR

NOTE 6: Absolute value of ZCK_t - ZCK_c

NOTE 7: Absolute value of TdCK_t - TdCK_c

NOTE 8: Single-ended impedance

NOTE 9: This value applies to QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR and QxCKE0/1, QxODT0/1, QxC2, QxCS[1:0]_n for Dual CS mode, QxCS[3:0]

NOTE 10: Absolute value of ZYn_t - ZYn_c

NOTE 11: Absolute value of TdYn_t - TdYn_c

NOTE 12: Absolute value of MAX(TdYn_t) - MIN(TdYn_t)

NOTE 13: This value applies to BCOM[3:0], BCKE and BODT

9 Timing requirements

Table 141 — Input Timing requirements

Symbol	Parameter	Conditions	DDR4-1600/ 1866/2133		DDR4-2400/2666		DDR4-2933/3200		
			Min	Max	Min	Max	Min	Max	Unit
f_{CLOCK}	Input clock frequency[1]	Application frequency[2]	625	1080	625	1350	625	1620	MHz
f_{TEST}	Input clock frequency	Test frequency[3]	140	625	140	625	140	625	MHz
t_{CH}/t_{CL}	Pulse duration, CK_t/CK_c HIGH or LOW		0.4	-	0.4	-	0.4	-	t_{CK}
$t_{jit\_inp(p-p)}$	Accumulated input phase jitter at CK_t/CK_c		0	50	0	50	0	50	ps
t_{ACT}	Inputs active time[4] before DRST_n is taken HIGH	DCKE0/1=LOW and DCS0/1_n=HIGH	16	-	16	-	16	-	t_{CK}
t_{MRD}	Control word to control word delay	Number of clock cycles between two control word accesses, MRS accesses, or any DRAM commands	8	-	8	-	8	-	t_{CK}
t_{MRD_L}	Control word to control word delay	Number of clock cycles between an access to F0RC03, F0RC04, F0RC05, F0RC0B DA0 and F0RC7x and the next control word access	16	-	16	-	16	-	t_{CK}
t_{MRD_L2}	Control word to control word delay	Number of clock cycles between an access to F0RC0F & F0RC0D and the next control word access or DRAM command[5]	32	-	32	-	32	-	t_{CK}
t_{MRD_PBA}	Control word to control word delay in PBA mode	Number of clock cycles between two control word accesses or any DRAM commands in PBA mode	See DDR4DB02 specification						t_{CK}
t_{MRC}	Register command word to CW or DRAM command delay	Number of clock cycles between register command word (F0RC06) and CW or any DRAM command	16	-	16	-	16	-	t_{CK}
t_{MRD1}	Control word to control word delay in gear-down mode	Number of clock cycles between two control word accesses, MRS accesses, or any DRAM commands	16	-	16	-	16	-	t_{CK}
t_{MRC1}	Register command word to CW or DRAM command delay in gear-down mode	Number of clock cycles between register command word (F0RC06) and CW or any DRAM command	32		32		32		t_{CK}
t_{CSALT}	Chip select assertion before and after ALERT_n Pulse Width de-assertion	Number of clock cycles between DCSx assertion and rising edge of ALERT_n when F0RC0E DA2 =1	8	-	8	-	8	-	t_{CK}
t_{InDIS}	Input buffers (except for CK_t/ CK_c, DCKEn, DODTn and DRST_n) disable time after DCKE[1:0] is LOW	DCKE[1:0] = LOW; DRST_n = HIGH; CK_t/ CK_c = Toggling; F0RC09[DA3]=1 and F0RC09[DA2]= 0 or 1	1	4	1	4	1	4	t_{CK}
t_{CKoff}	Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK_t/CK_c are driven LOW	DCKE[1:0] = LOW; DRST_n = HIGH; CK_t/ CK_c = Toggling	5+CLA[6]	-	5+CLA[6]	-	5+CLA[6]	-	t_{CK}
t_{CKEV}	Input buffers (DCKE0 and DCKE1) disable time after CK_t/CK_c = LOW	DCKE[1:0] = LOW; DRST_n = HIGH; CK_t/ CK_c = LOW	4	-	6	-	8	-	t_{CK}
$t_{Fixedoutput}$	Static register output after DCKE0 or DCKE1 is HIGH at the input (exit from Power saving state)	F0RC09[DA3]=1 and F0RC09[DA2]=0 or 1	1	3+CLA[6]	1	4+CLA[6]	1	5+CLA[6]	t_{CK}
tZQInit	Power-up and RESET calibration time		1024		1024		1024		t_{CK}
tZQOper	Normal operation long calibration time		512		512		512		t_{CK}
tZQCS	Normal operation short calibration time		128		128		128		t_{CK}

1. Including SSC according Table 133, “SSC and PLL Loop Filter Characteristics,”.
2. All specified timing parameters apply
3. Timing parameters specified for frequency band 2 apply
4. This parameter is not necessarily production tested.
5. This parameter also applies to DDR4DB02 BCWs F0BC06, F0BC07, F0BC0A, F0BC0C, F0BC1x, F0BC6x, F[3:0]BC2x/3x,F[3:0]BC4x/5x, F[3:0]BC8x/9x, F[3:0]BCAx/Bx, F[7:4]BC8x/9x, F[7:4]BCAx/Bx, F[7:4]BCCx/Dx/Ex/Fx and F5BC4x.
6. CLA = Command Latency Adder from F0RC0F

Table 142 — Output timing requirements[1]

Symbol	Parameter	Conditions	Min	Max	Unit
t_{PDM}[2]	Propagation delay, single bit switching; CK_t/CK_c cross point to output	1.2 V Operation	1.0	1.3	ns
t_{ALERT}	ALERT_n propagation delay	ERROR_IN_n LOW to ALERT_n LOW	-	2	ns
t_{ALERT_HL}	ALERT_n assertion delay from CK_t/CK_c	CK_t/CK_c to ALERT_n LOW[3]	-	1.5	ns
t_{RST}	RESET propagation delay	DRST_n LOW to QRST_n LOW	-	20	ns
t_{QDIS}	Output buffers (except for Yn_t/Yn_c, QxCKEn, QxODTn) hi-z after QxCKEn is driven LOW	DCKE[1:0] = LOW; DRST_n = HIGH; CK_t/CK_c = toggling; F0RC09[DA3]=1 and F0RC09[DA2]=0 or 1	4.5	-	t_{CK}
t_{DIS}	Output disable[4] time	Rising edge of Yn_t to output float[5]	0.5*tCK + tQSK1(min)	-	ps
t_{EN}	Output enable[6] time	Output valid[5] to rising edge of Yn_t	0.5*tCK - tQSK1(max)	-	ps
t_{ODU}	Output Delay Update [7] time	DA7 = 1 for F1RC1x to F1RC9x	-	100	ns

1. See diagram (Figure 79, “Reference Load for AC Timing and Output Slew Rate” on page 171)
2. See diagram (Figure 68, “Propagation Delay Timing” on page 161). t_{PDM} is defined for 0 nCK command latency adder (F0RC0F bits DA[2:0] = ‘100’), default (Moderate) output slew rate control settings in F1RC02 - F1RC05, and output delay features all disabled in F1RC1x - F1RC9x.
3. See Figure 77, “Load circuit, ALERT_n Outputs” on page 170 and Figure 78, “Voltage waveforms, tALERT_HL Measurement” on page 170.
4. This is the time the output requires to switch from normal impedance to the impedance defined by the weak drive mode when all DCS[n:0]_n are latched in HIGH. This could be floating or high impedance driving. The corresponding reference clock edge is determined by the first occurrence of all QxCS[n:0]_n HIGH. This timing is also valid for entering the CKE power down mode
5. See diagram (Figure 75, “Voltage waveforms address floating” on page 168)
6. This is the time the output requires to switch from weak drive to normal impedance defined by the weak drive mode when one or more DCS[n:0]_n are latched in HIGH. The reference clock edge for the measurement is determined by the first occurrence of the respective QxCS[n:0]_n LOW. This timing is also valid for leaving the CKE power down mode except that in this case the referencing clock edge is determined by the first occurrence of any or both QxCKE0/1 HIGH
7. This is the time the RCD02 requires to update delay timing setting to the output after it receives CW write operation CMD 5.

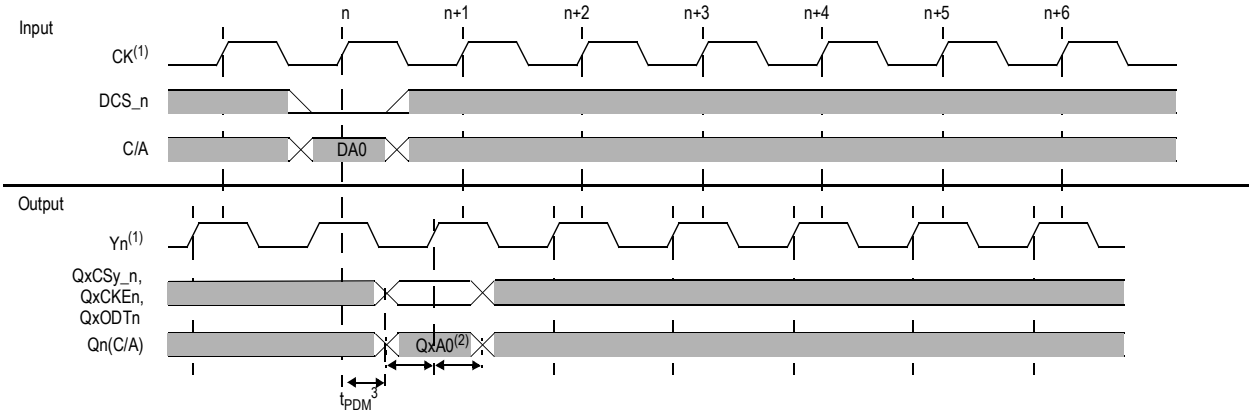


Figure 68 — Propagation Delay Timing

1. CK_c and Yn_c left out for better visibility
2. QxA0 is re-driven command address output based on input DA0
3. t_{PDM} is defined for 0 nCK command latency adder (F0RC0F bits DA[2:0] = 100)

Table 143 — Control Gear-down Mode Timing Parameters

Symbol	Parameter	Conditions	DDR4-2666		DDR4-2933		DDR4-3200		Unit
			Min	Max	Min	Max	Min	Max	
$t_{Sync\ RCD\_GEAR}$	The time from last Nop to F0RC06 CGM entry		8	-	8	-	8	-	
$t_{CMD\_RCD\_GEAR}$	The time of 2N normal operation after F0RC06 CGM CMD is received[1]		24	-	24	-	24	-	t_{CK}
t_{InDIS_GEAR}	Input buffers (except for CK_t/CK_c, DCKEn, DODTn and DRST_n) disable time after DCKE[1:0] is LOW	DCKE[1:0] = LOW; DRST_n = HIGH; CK_t/CK_c = Toggling; F0RC09[DA3]=1 and F0RC09[DA2]= 0 or 1	2	4	2	4	2	4	t_{CK}
t_{CKoff_GEAR}	Number of tCK required for both DCKE0 and DCKE1 to remain LOW before both CK_t/CK_c are driven LOW	DCKE[1:0] = LOW; DRST_n = HIGH; CK_t/CK_c = Toggling	6.5 + CLA	-	6.5 + CLA	-	6.5 + CLA	-	
t_{QDIS_GEAR}	Output buffers (except for Yn_t/Yn_c, QxCKEn, QxODTn) hi-z after QxCKEn is driven LOW on active rising transition of Yn_t/Yn_c	DCKE[1:0] = LOW; DRST_n = HIGH; CK_t/CK_c = toggling; F0RC09[DA3]=1 and F0RC09[DA2]=0 or 1	5	-	5	-	5	-	t_{CK}
$t_{Fixedoutput\_GEAR}$	Static register output after DCKE0 or DCKE1 is HIGH at the input (exit from Power saving state)	F0RC09[DA3]=1 and F0RC09[DA2]=0 or 1	2	4 + CLA	2	6 + CLA	2	6 + CLA	t_{CK}

1. This parameter has to be even number of clocks.

10 I²C Electrical and Timing Specifications

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the DDR4RCD02 I²C interface. The parameter in the DC and AC Characteristics tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuits match the measurement conditions when relying on the quoted parameters.

Table 144 — Operating Conditions for the I²C Bus Interface

Symbol	Parameter	Min	Max	Unit
V_{DDSPD}	I²C Bus Supply Voltage	2.2	2.8	V

Table 145 — AC Measurement Conditions for I²C BUS interface

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times	--	50	ns
	Input levels	0.2 * V_{DDSPD} to 0.8 * V_{DDSPD}		V
	Input and output timing reference levels	0.3 * V_{DDSPD} to 0.7 * V_{DDSPD}		V

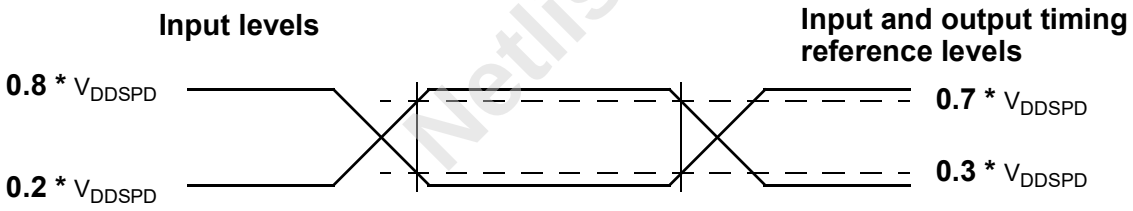


Figure 69 — AC Measurement I/O Waveform

Table 146 — Input Parameters for I²C Bus interface

Symbol	Parameter[1,2]	Test Condition	Min	Max	Unit
C_{IN}	Input capacitance (SDA)	--	--	5	pF
C_{IN}	Input capacitance (other pins)	--	--	5	pF
Z_{EIL}	Ei (SA0, SA1, SA2) input impedance	V_{IN} < 0.3 * V_{DDSPD}	30	--	kΩ
Z_{EIH}	Ei (SA0, SA1, SA2) input impedance	V_{IN} > 0.7 * V_{DDSPD}	800	--	kΩ

NOTE 1: TA = 25 °C, f = 1000 kHz
NOTE 2: Verified by design and characterization, not necessarily tested on all devices

Table 147 — DC Characteristics for I^2C Bus interface

Symbol	Parameter	Test Condition (in addition to those in Table 144 on page 163)	Min	Max	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{DDSPD}	--	±5	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ or V_{DDSPD}, SDA in Hi-Z	--	±5	µA
I_{DDSPD}	Supply current	V_{DDSPD} = 2.5 V, f_C = 1000 kHz (rise/fall time < 30 ns)	--	5	mA
I_{DDSPD1}	Standby Supply current	$V_{IN} = V_{SS}$ or V_{DDSPD}, V_{DDSPD} = 2.5 V	--	100	µA
V_{IL}	Input low voltage (SCL, SDA, SA[2:0])	--	-0.5	0.3 * V_{DDSPD}	V
V_{IH}	Input high voltage (SCL, SDA, SA[2:0])	--	0.7 * V_{DDSPD}	V_{DDSPD}+ 0.5	V
V_{HV}[1]	SA0 high voltage		7	10	V
V_{IL_BFUNC}	Input low voltage (BFUNC)	--	V_{SS}[2]	0.35 * V_{DD}	V
V_{IH_BFUNC}	Input high voltage (BFUNC)	--	0.65 * V_{DD}	V_{DD}[3]	V
V_{OL}	Output low voltage	20 mA sink current	--	0.4	V
I_{OL}	LOW-level output current	V_{OL} = 0.4V	20	--	mA
V_{HYST}	Input hysteresis		0.05 * V_{DDPD}	--	V

NOTE 1: V_{HV} is used by the SPD device. For DDR4 RDIMM or LRDIMM, a series resistor is connected to the DDR4RCD02 input (refer to Figure 32 in the I^2C Bus chapter). As such, the voltage drop across the external series resistor prevents the SA0 input of the DDR4RCD02 from being directly exposed to dangerous voltage levels.
NOTE 2: Undershoot might occur. It should be limited by the Absolute Maximum DC Ratings.
NOTE 3: Overshoot might occur. It should be limited by Absolute Maximum DC Ratings

Table 148 — AC Characteristics for I^2C Bus interface

Symbol	Parameter	≤ 400 kHz		> 400 kHz		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock frequency	10	400	401	1000	kHz
t_{HIGH}	Clock pulse width high time	600		260	--	ns
t_{LOW}[3]	Clock pulse width low time	1300		500	--	ns
$t_{TIMEOUT}$[4,5]	Detect clock low timeout	45		45	--	ms
t_R[2]	SDA rise time		300	--	120	ns
t_F[2]	SDA fall time		300	--	120	ns
$t_{SU:DAT}$	Data in setup time	50	--	50	--	ns
$t_{HD:DI}$	Data in hold time	0	--	0	--	ns
$t_{HD:DAT}$	Data out hold time	0	350	0	350	ns
$t_{SU:STA}$[1]	Start condition setup time	260	--	260	--	ns
$t_{HD:STA}$	Start condition hold time	260	--	260	--	ns
$t_{SU:STO}$	Stop condition setup time	260	--	260	--	ns
t_{BUF}	Time between Stop Condition and next Start Condition	500	--	500	--	ns

NOTE 1: For a reSTART condition, or following a write cycle
NOTE 2: Guaranteed by design and characterization, not necessarily tested
NOTE 3: The DDR4RCD02 I^2C Bus interface logic shall not initiate clock stretching
NOTE 4: The DDR4RCD02 must support bus timeout on I^2C Bus access.
NOTE 5: Devices participating in a transfer can abort the transfer in progress and release the bus by forcing SCL LOW. A timeout condition can only be ensured if the device forcing the timeout holds SCL LOW for $t_{TIMEOUT,MIN}$ or longer. After the master in a transaction detects this condition, it must generate a STOP condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than 10ms after the master generates the STOP condition.

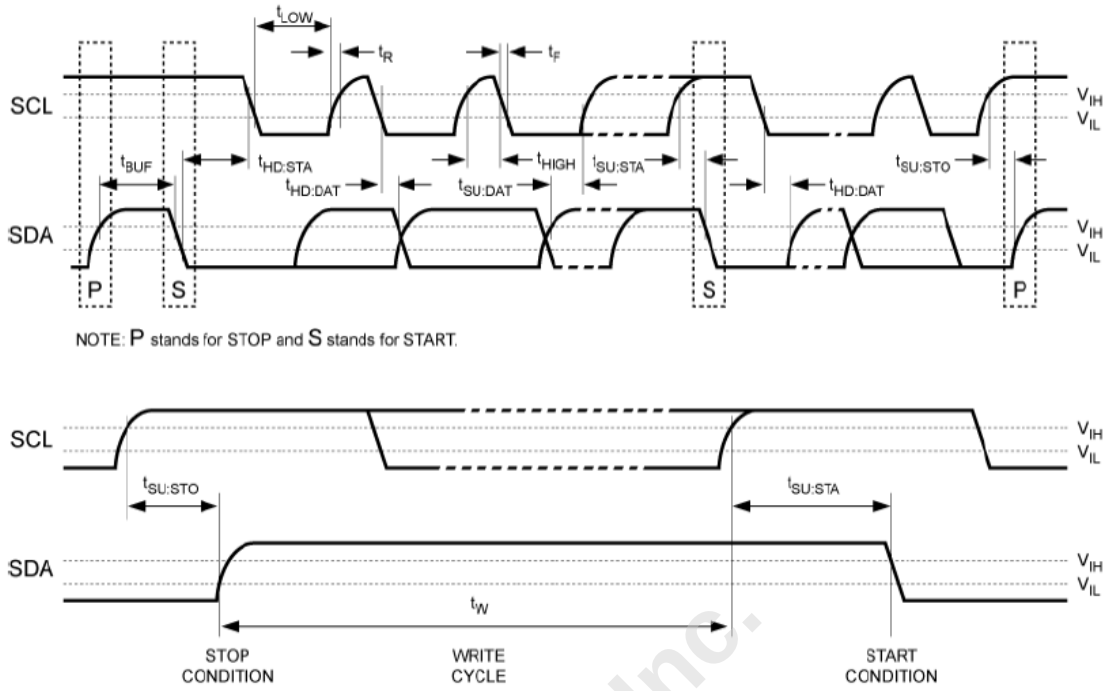


Figure 70 — I^2C Bus AC Waveforms

11 Test circuits and switching waveforms

11.1 Parameter measurement information

All input pulses are supplied by generators having the following characteristics: 625 MHz ≤ PRR ≤ 1620 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.

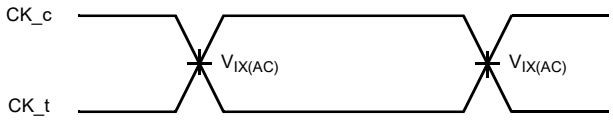


Figure 71 — Voltage waveforms; input clock

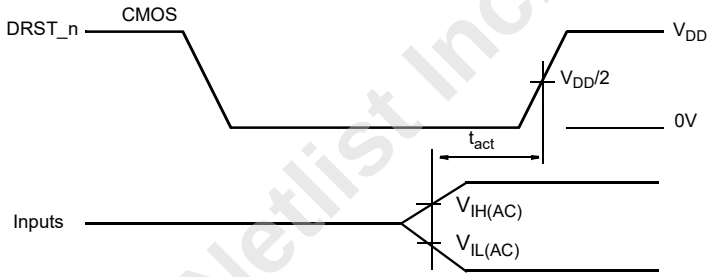
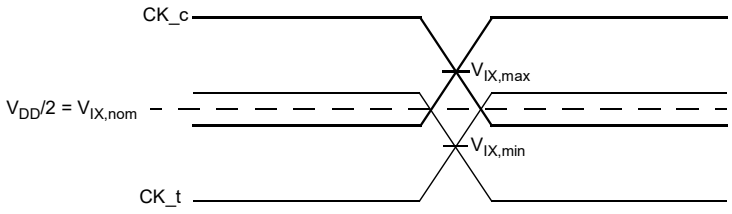


Figure 72 — Voltage and current waveforms; inputs active and inactive times



For V_{IX} Range testing common mode voltage of CK_t and CK_c is shifted around $V_{DD}/2$. Functional Tests are performed with this V_{IX} shift.

Figure 73 — Input Waveforms V_{IX} range measurement

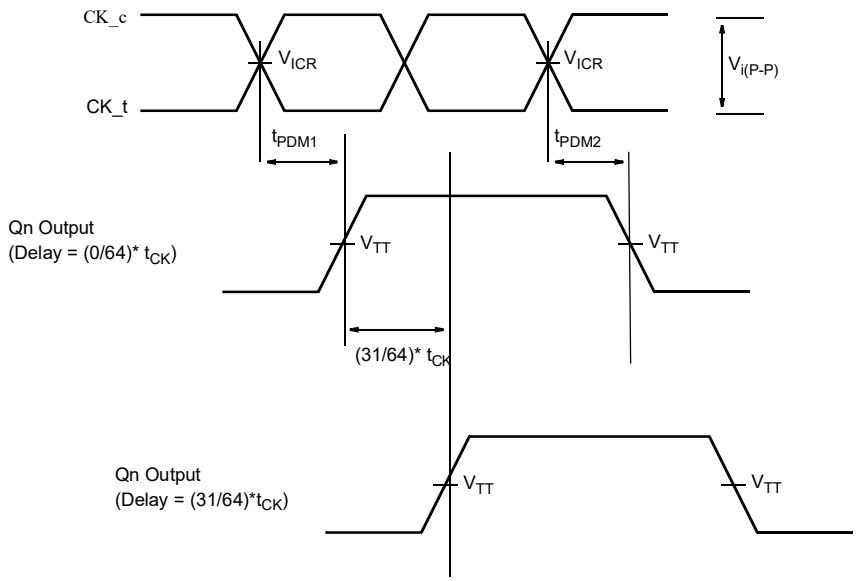


Figure 74 — Voltage waveforms; propagation delay times

V_{ICR} Cross Point Voltage
$V_{i(P-P)}$ = 400mV (1.2 V Operation)
t_{PDM1}, t_{PDM2} the larger number of both has to be taken when performing t_{PDM} max measurement, the smaller number of both has to be taken when performing t_{PDM} min measurement

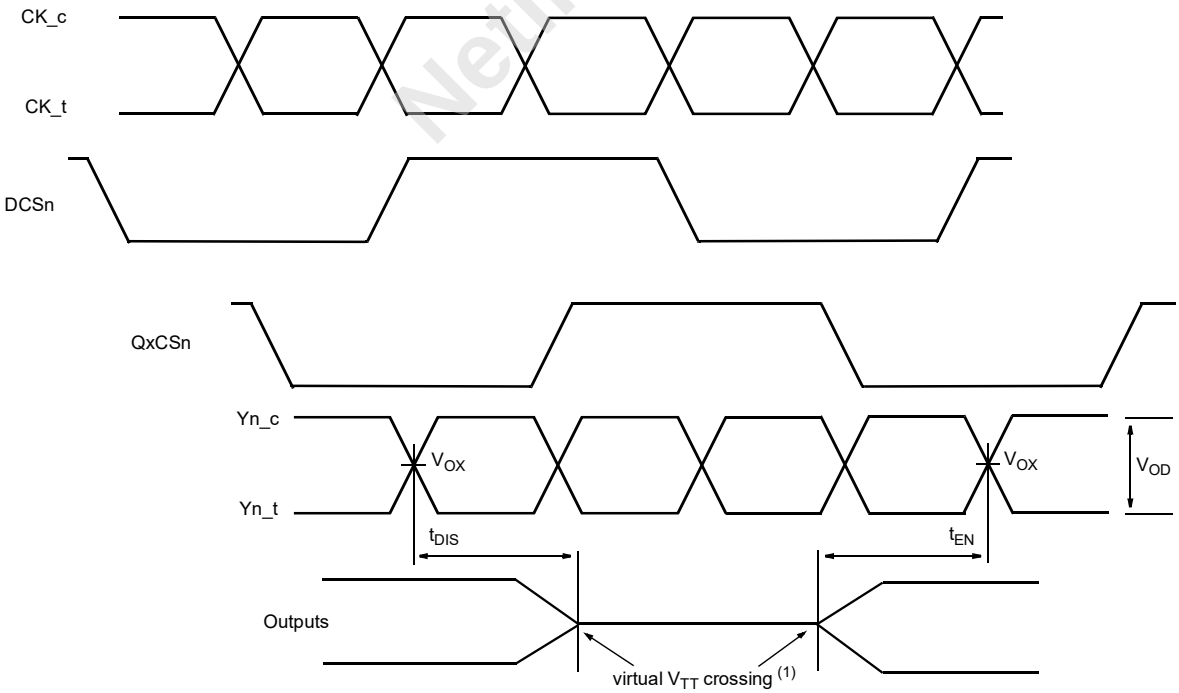
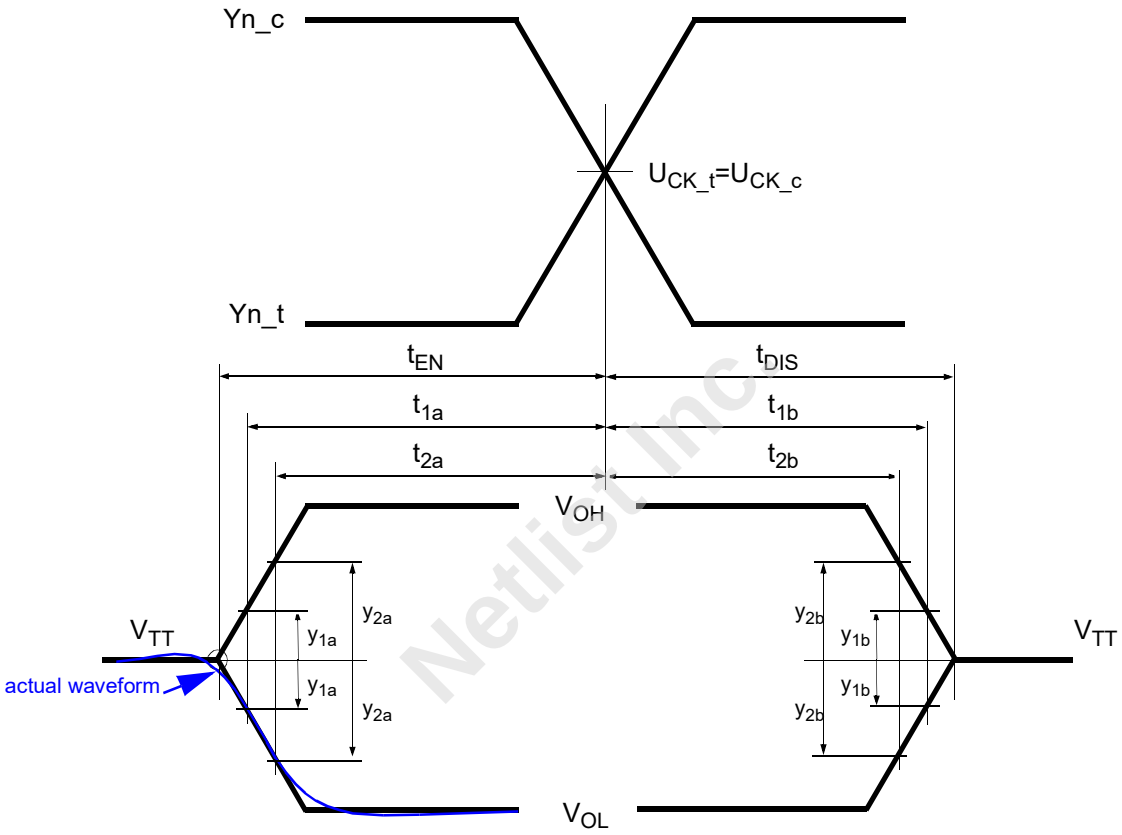


Figure 75 — Voltage waveforms address floating

(1) See Figure 76

Enabling and disabling the CA outputs must not violate DRAM setup and hold time requirements. Therefore a t_{DIS} transition may not occur earlier than the earliest (HL/LH) transition and a t_{EN} transition may not occur later than the latest (HL/LH) transition. Regular transitions are measured between CK_t/CK_c and CA/V_{TT} crossings. However a V_{TT} crossing is not available in the state where the outputs are Hi-Z. To allow a correct and not overly conservative measurement a virtual V_{TT} crossing point is defined below. The calculation of the virtual V_{TT} crossing point is shown in Figure 76. The voltage levels for y1a, y2a, y1b and y2b are measured from V_{TT} (V_{DD}/2) and should be selected such that the region between t1 and t2 covers a linear range and represents a typical slope of the waveform within the transition area. They have to be used signed in the formula.



$t_{EN} = t_{1a} + y_{1a}(t_{1a}-t_{2a})/(y_{2a}-y_{1a})$ $t_{DIS} = t_{1b} + y_{1b}(t_{1b}-t_{2b})/(y_{2b}-y_{1b})$

Figure 76 — Calculating the virtual V_{TT} crossing point

11.2 Alert output load circuit and voltage measurement information

All input pulses are supplied by generators having the following characteristics: 625 MHz ≤ PRR ≤ 1620 MHz;

Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

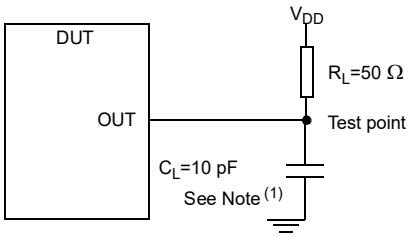


Figure 77 — Load circuit, ALERT_n Outputs

(1) C_L includes probe and jig capacitance.

Output driver characteristics are separately controlled for outputs that are often loaded with twice as many DRAMs as the other outputs. Outputs are grouped as follows:

- CA Signals = QxA0..QxA17, QxBA0..QxBA1, QxBG0..QxBG1, QxACT_n, QxC2, QxPAR
- Control Signals = QxCKE0/1, QxODT0/1, QxC2, QxCS[1:0]_n for Dual CS mode, QxCS[3:0]
- CK = Yn_t - Yn_c

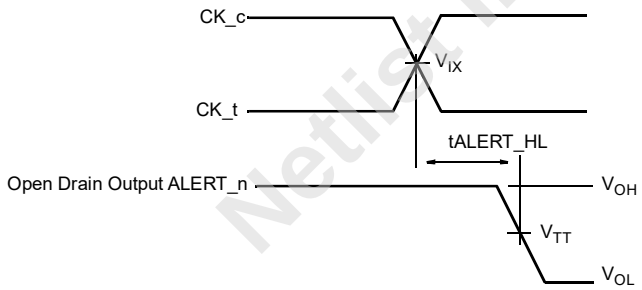


Figure 78 — Voltage waveforms, tALERT_HL Measurement

11.3 DDR4 Register Reference Load

The following circuit represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or

more coaxial transmission lines terminated at the tester electronics.

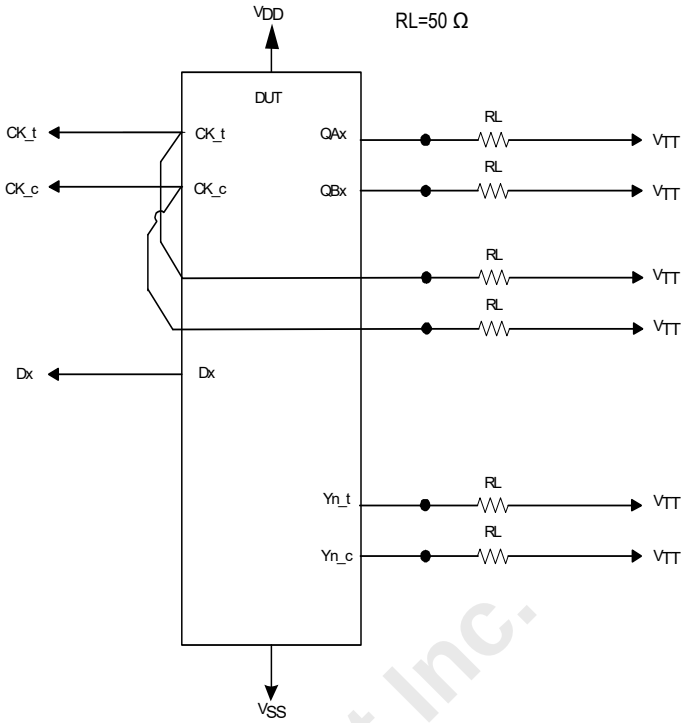


Figure 79 — Reference Load for AC Timing and Output Slew Rate

12 Recommended Filtering for the Analog Power supply (AV_{DD})

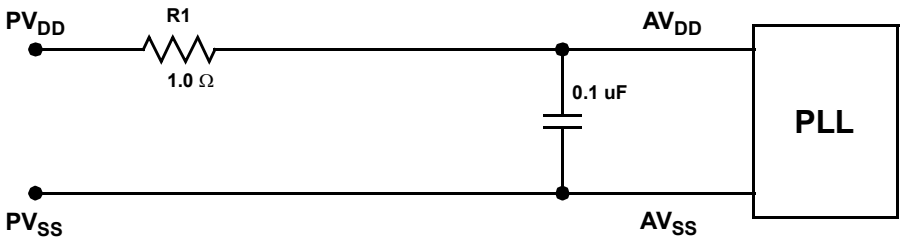


Figure 80 — AV_{DD} Filtering

V_{DD} and V_{SS} via comprise AV_{DD} filter network should not have connections to V_{DD} and V_{SS} on outer layers. On the outer layers the vias only connect to filter components and AV_{SS} of register.

13 LCOM Electrical and Timings

If the optional NVDIMM mode feature is supported, the LCOM interface is available in the RCD02. The LCOM functionality is described in the DDR4RCD02 LCOM protocol and RCW definition, and the LCOM electrical interface and timing is described in this section.

13.1 Transmitter

The output drivers for the LCOM[1:0] bidirectional pins operate as described here.

LCOM[1:0] RONpu and RONpd are 50Ω +/-15%

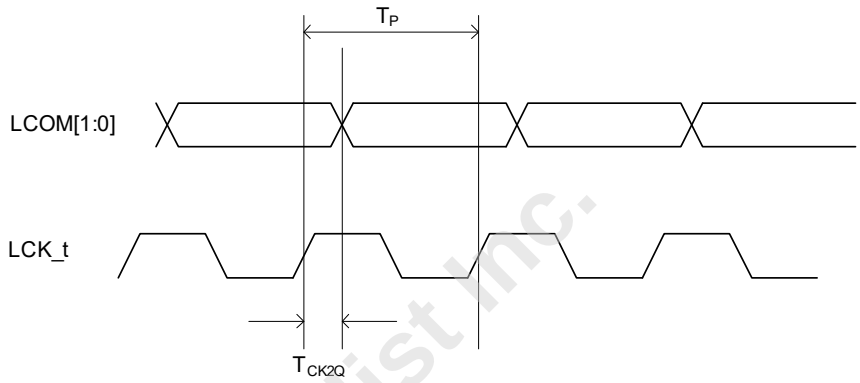


Figure 81 — LCOM[1:0] Output Timing

Table 149 — LCOM[1:0] Output Timing Parameters

Symbol	Parameter	Min	Max	Unit
T_P	Period	2	5	ns
t_{CK2Q}	Clock to Output	–	1.6	ns

13.1.1 Single-Ended LCOM[1:0] Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLNV(AC)}$ and $V_{OHNV(AC)}$ for the LCOM[1:0] single-ended signals as shown in Table 150, Table 151 and Figure 82.

Table 150 — LCOM[1:0] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	$[V_{OH(AC)} - V_{OL(AC)}]$ / DeltaTFse
NOTE Output slew rate is verified by design and characterization, and may not be subject to production test.			

Table 151 — LCOM[1:0] Output Operating Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
$V_{OHNV(AC)}$	AC output high level	$0.75*V_{DD} + 0.15*V_{DD}$	–	V
$V_{OLNV(AC)}$	AC output low level	–	$0.75*V_{DD} - 0.15*V_{DD}$	V
1. NVC $V_{REF} = 0.75*V_{DD}$				

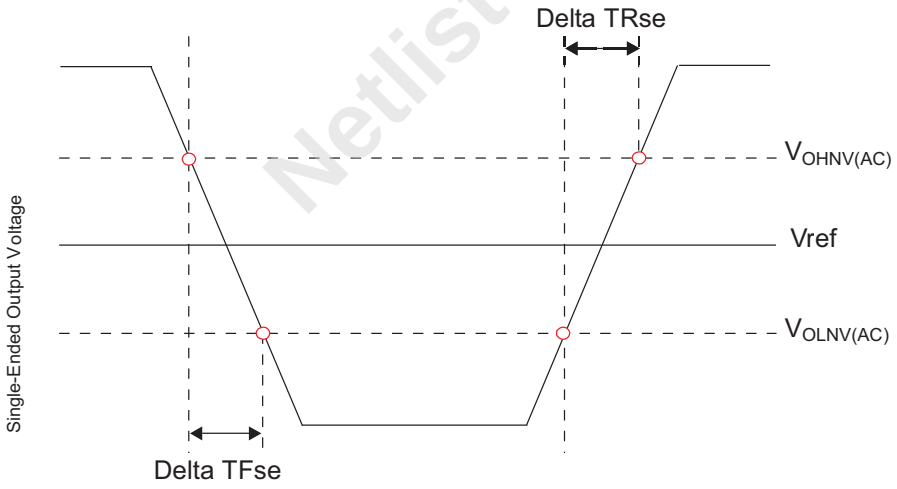


Figure 82 — LCOM[1:0] Single-Ended Output Slew Rate Definition

Table 152 — LCOM Single-Ended Output Edge Rates Over Specified Operating Temperature Range

Symbol	Parameter[1]	Conditions	Min	Max	Unit
dV/dt_r	rising edge slew rate[2]	1.2V operation	1	8	V/ns
dV/dt_f	falling edge slew rate[2]	1.2V operation	1	8	V/ns
dV/dt_D[3]	absolute difference between dV/dt_r and dV/dt_f	–	-	1	V/ns

1. These parameters are for the LCOM[1:0] output drivers.
2. Measured into reference load in Figure 84.
3. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

13.1.2 LCOM[1:0] Output Drive Parameters

The output impedance RON is defined by the value of the external reference resistor as defined in Table 153.

Table 153 — LCOM[1:0] Output Driver DC Electrical Characteristics

RON_{Nom}	Resistor	Vout	Min	Nom	Max	Unit (Ω)
50 Ω	RON_{50Pd}	$V_{OLdc} = 0.6 \times V_{DD}$	0.6	1.0	1.15	50
		$V_{OMdc} = 0.75 \times V_{DD}$	0.85	1.0	1.15	50
		$V_{OHdc} = 0.9 \times V_{DD}$	0.85	1.0	1.4	50
	RON_{50Pu}	$V_{OLdc} = 0.6 \times V_{DD}$	0.85	1.0	1.4	50
		$V_{OMdc} = 0.75 \times V_{DD}$	0.85	1.0	1.15	50
		$V_{OHdc} = 0.9 \times V_{DD}$	0.6	1.0	1.15	50

A functional representation of the output buffer is shown in Figure 83.

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{V_{DD} - V_{Out}}{|I_{Out}|}$$ Under the condition that RON_{Pd} is turned off

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ Under the condition that RON_{Pu} is turned off

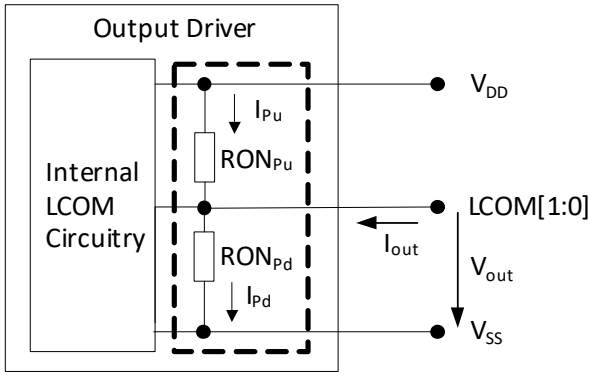


Figure 83 — LCOM[1:0] Output Driver: Definition of Voltages and Currents

13.1.3 LCOM[1:0] Reference Load

The following circuit represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

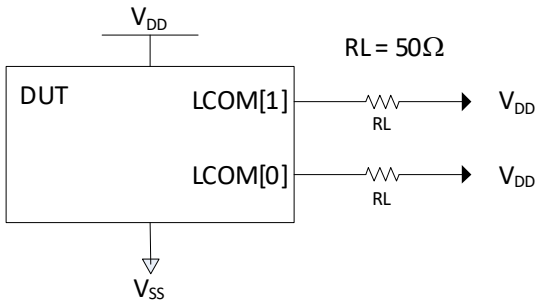


Figure 84 — Reference Load for AC Timing and Output Slew Rate

13.2 Receiver

The receiver for each LCOM interface input pin operates as described here.

LCKE, LCOM[2] and LCOM[1:0]:

- Termination and Reference Voltage:
  - Assumption: the NVC driver RON is 50Ω
  - 50Ω +/-15% to V_{DD}, with Vref = 0.75 * V_{DD}
  - 100Ω +/-15% to V_{DD}, with Vref = 0.65 * V_{DD}
  - Unterminated, with Vref = 0.5 * V_{DD}
  - Refer to F4RC03 and F4RC04: LCKE, LCOM[2] and LCOM[1:0] Receiver Configuration
- V_{IL} and V_{IH}: Vref +/- 0.1 * V_{DD}

LCOM t_{SU} and t_H in Figure 85 and Table 154 are measured from the crossing point between the rising transition of LCK_t, and the falling transition of LCK_c, to the points where LCOM rising or falling transitions cross with vref.

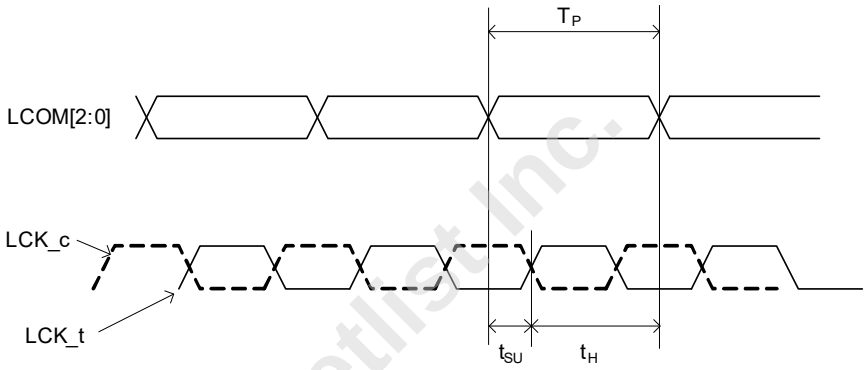


Figure 85 — LCOM Receiver Timing

Table 154 — LCOM Receiver Timing Parameters

Symbol	Parameter	Min	Max	Unit
T_P	Period	2	5	ns
t_{SU}	Setup	400	-	ps
t_H	Hold	400	-	ps

1. This table describes the parameters in the timing diagram in Figure 85.
2. See Section 13.2.2 "Single-Ended Requirements for LCK_t/LCK_c " on page 178 for the LCK V_{REF}.

13.2.1 LCOM Receiver Termination

Signals: LCOM[2], LCOM[1], LCOM[0], and LCKE

RX termination: 50Ω, 100Ω, and Unterminated

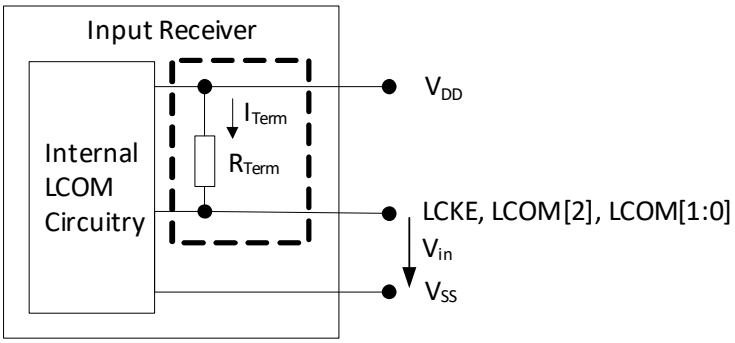


Figure 86 — LCOM Input Receiver

13.2.2 Single-Ended Requirements for LCK_t/LCK_c

Each individual component of the differential signal LCK_t/LCK_c must also comply with certain requirements for single-ended signals.

LCK_t and LCK_c have to approximately reach V_{SEH} min / V_{SEL} max (equal to the AC-levels ($V_{IH(AC)}$ / $V_{IL(AC)}$)) in every half-cycle. $V_{IH(AC)} = V_{DD}/2 + 0.1*V_{DD}$, and $V_{IL(AC)} = V_{DD}/2 - 0.1*V_{DD}$.

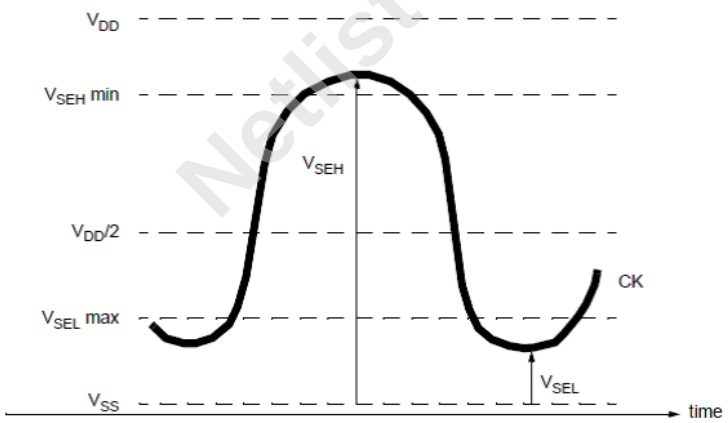


Figure 87 — Single-ended Requirement for Differential Signals

The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals, the requirement to reach V_{SEL} max, V_{SEH} min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 155 — Single-ended Levels for LCK_t/LCK_c

Symbol	Parameter	Min	Max	Unit
V_{SEH}	Single-ended high-level for LCK_t/LCK_c	$(V_{DD}/2) + 0.1*V_{DD}$	Note	mV
V_{SEL}	Single-ended low-level for LCK_t/LCK_c	Note	$(V_{DD}/2) - 0.1*V_{DD}$	mV

NOTE 1: These values are not defined, however the single-ended signals LCK_t and LCK_c need to be within the limitations for overshoot and undershoot.

14 Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Products*
JEP104, *Reference Guide to Letter Symbols for Semiconductor Devices.*
JESD21-C, *Configuration for Solid State Memories.*
JESD8-11A, *Definition of wide range non-terminated logic*
JESD79-4, *DDR4 SDRAM Specification*
DDR4DB02 Specification
MO-307A, *Package Mechanical Outline*
Byte Addressable Energy Backed Interface, Version 2.0

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